WAVETEK

SIGNAL GENERATOR
MODEL 2500
SERVICE MANUAL

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USE OF THIS MANUAL

The documentation package for the Wavetek Model 2500 Signal Generator consists of an Operating Manual and a Service Manual. This is the Service Manual. It contains Sections 8 through 11 of the documentation package.

Section 8 Contains a detailed Theory of Operation for the instrument.

Section 9 Provides Troubleshooting information for the instrument.

Section 10 Contains the Replaceable Parts Lists, Schematics, Parts Layouts, and Assembly reference drawings. Schematics and their associated Parts Layout drawings are bound together.

Section 11 Contains any changes that must be made to the Service Manual. Wavetek's product improvement program incorporates the most current technology as rapidly as development and testing will permit. Due to the time required to document and print Operating/Service manuals, it is not always possible to include information about product improvements in the original printing for a manual. Engineering updates to address these changes occur in Section 11.

Please note that each of the figures in the text and each reference drawing in Section 11 has a ten digit identification number (xxxx-xx-xxxx). These numbers are for internal use by Wavetek. For example, Figure 8-2 carries Wavetek identification number 6510-01-0036.

The Operating Manual supplied with the instrument contains the first seven sections of the documentation package.

Section 1 Provides general information about the unit, including specifications.

Section 2 Contains detailed installation instructions.

Section 3 Provides operating instructions for the unit.

Section 4 Contains the performance tests used to verify the unit works properly.

Section 5 Contains the maintenance instructions for the unit, including calibration procedures.

Section 6 Provides GPIB documentation.

Section 7 Contains any changes that must be made to the Operating Manual.

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8.1 INTRODUCTION

The block diagram showing signal generation in the Model 2500 Synthesized Signal Generator is shown in Figure 8-1. The unit will be broken into the basic circuitry groups shown. An overview of each group and the power supply (not shown in Figure 8-1) will be presented, followed by more detailed circuit descriptions where appropriate. The schematics in Section 10 of this Service Manual will be referred to extensively in the following discussions.

System frequency references (internal and external) are shown in the lower left hand section of Figure 8-1. Modulation circuitry (internal and external) is shown at the bottom of Figure 8-1. The basic frequency synthesis circuitry includes the Direct Digital Synthesis (DDS) section, the Single Side Band (SSB) Mixer, the Main Loop Frequency Divider, and the components shown in the Oscillator Assembly. The Amplifier Assembly contains the frequency conversion circuitry, an Output Amplifier, and Leveler circuitry. Finally, the Programmable Attenuator and Reverse Power Protection are shown.

8.2 OVERVIEW - INTERNAL/EXTERNAL REFERENCES AND MODULATION

8.2.1 The internal/external reference switching circuitry is select logic that determines whether the internal 10 MHz Temperature Compensated Crystal Oscillator (TCXO) source will be used as the frequency reference or an external 1 MHz, 5 MHz, or 10 MHz source will be substituted.

The 10 MHz internal reference is applied to a jack on the rear panel, as shown in Figure 3-2 of the Operating Manual.

8.2.2 The selected reference signal (internal or external) is applied to the reference divider and modulation source circuitry. This circuitry provides internal 400 Hz and 1000 Hz modulation sources. It also provides the 1 MHz reference signal to the phase detectors in the Oscillator Assembly and the Direct Digital Synthesis (DDS) section.

8.2.2.1 The internal modulation sources are fed through a low pass filter section into the internal modulation level control circuitry.

8.2.3 External Modulation is amplified/buffered and then applied to the External Modulation Level Control circuitry.

8.2.4 The Modulation Routing Section receives inputs from both internal and external level control circuits and selects the Modulation Mode or combination of Modulation Modes used.

8.2.4.1 The Modulation Routing Section sends Amplitude Modulation (AM) information to the Carrier Level and % Modulation Control circuitry for further processing. This processed signal provides the reference for the Leveler circuitry in the Amplifier Assembly.

8.2.4.2 The Modulation Routing Section also sends Frequency Modulation (FM) information to the FM Deviation Correction and Range Switching circuitry.

Processed information is sent to the FM control section of the Oscillator Assembly.

8.3 OVERVIEW - FREQUENCY SYNTHESIS

8.3.1 The Oscillator Assembly contains two phase detectors (Ø) each of which receives a 1 MHz reference signal from the Reference Divider and Modulation Source Circuitry.

8.3.2 The Local Oscillator Loop in the Oscillator Assembly provides a 500 MHz output to the Mixer in the Amplifier Assembly.

8.3.2.1 The 500 MHz output from this loop also is fed to a divide-by-500 (÷ 500) circuit.

8.3.2.2 The resultant 1 MHz signal (500 MHz ÷ 500 = 1 MHz) is applied to the phase detector to provide an error voltage, as appropriate, to lock the loop output at 500 MHz.

8.3.3 The Main Loop in the Oscillator Assembly contains four VCOs that provide outputs from 275 - 550 MHz (in 4 ranges as shown) to the associated Amplifier Assembly frequency conversion circuitry.

8.3.3.1 Main loop output frequency is the product of several operations. Software selects the appropriate VCO from the VCO group. Software also provides the appropriate word (10 bits) to the Coarse Tuning circuitry to generate an output frequency within tracking (lock-in) range of the loop.

8.3.3.2 Frequency lock-in is controlled by the feedback circuit from the Main Loop output to the phase detector in the Main Loop.

8.3.3.3 The output from the Main Loop in the Oscillator Assembly is fed to the Single Side Band (SSB) Mixer and then to the Main Loop Frequency Divider.

8.3.3.4 The SSB Mixer also receives inputs from its associated DDS section and controls frequency output/changes of the 10 Hz to 10 kHz digits. (For example, the "37" part of the frequency 301.937 MHz is locked by the SSB Mixer/ DDS circuitry.)

8.3.3.5 The Main Loop Frequency Divider controls frequency output/changes of the 100 kHz to 100 MHz digits. (In the above example, the "301.9" part of the frequency 301.937 MHz is locked by the Main Loop Frequency Divider circuitry.)

8.3.3.6 Each loop in the Oscillator Assembly contains filter circuitry as shown.

8.3.3.7 The Main Loop also contains Error Indicating circuitry (Unlock/ Overdeviation Detection) and Automatic Phase Control (APC) Comparator circuitry. (The APC Comparator circuitry is used during the AutoCal® procedure.)

8.4 OVERVIEW - FREQUENCY CONVERSION

8.4.1 The 500 MHz output from the Local Oscillator loop of the Oscillator Assembly and the basic frequency output synthesized in the Main Loop of the Oscillator Assembly are fed to frequency conversion circuitry in the Amplifier Assembly. Oscillator Assembly outputs are processed in the Amplifier Assembly according to the setting of its switch as shown.

8.4.2 If the Amplifier Assembly switch is at the topmost position shown on Figure 8-1, the main loop VCO output will be heterodyned with the Local Oscillator VCO output to produce a 400 kHz - 137.5 MHz signal to be applied to the Output Amplifier.

8.4.3 If the Amplifier Assembly switch is connected to the divide by two (÷ 2) circuitry, the main loop VCO output will be divided by two, applying 137.5 - 275 MHz to the Output Amplifier.

FO Figure 8-1 (0013-30-0006)

8-3

Back of FO Figure 8-1

8.4.4 The third switch position (in a clockwise direction from the topmost position shown) provides direct coupling of the main loop VCO output to the Output Amplifier (275 - 500 MHz).

8.4.5 The last position on the Amplifier Assembly switch connects the main loop VCO output to a frequency doubler circuit to provide a 550 - 1100 MHz input to the Output Amplifier.

8.4.6 The signal pathways in the Amplifier Assembly contain switched lowpass and switched bandpass filters as shown.

8.5 DETAILED THEORY OF OPERATION

The following circuit descriptions make extensive references to the schematic diagrams bound in Section 10 of this Service Manual. Schematics and their associated parts layout diagram(s) are located together in Section 10. Relative locations of the circuit boards, modules, and programmable attenuator are shown in Figures 8-2 through 8-4.

Chassis wiring for the Model 2500 Signal Generator is shown in Figure 10-1. This reference drawing and the block diagram of Figure 8-1 provide a clear picture of the relationship between the major circuitry sections of the Model 2500.

Each circuit board or module will have a separate section of text. The text describes each board/module in terms of the schematic(s) associated with the assembly. Some have more than one schematic. The Main Board, for example, has four schematics (see schematic drawing 0014-30-0348, 4 sheets; Figures 10-2 through 10-5). These contain the internal/external reference circuitry, internal/external modulation circuitry, and the frequency synthesis circuitry.

8.5.1 MAIN BOARD, MOD SOURCE/REF FREQ

The Main Board internal/external reference circuitry is shown on the Mod Source/Ref Freq schematic, reference drawing 10-2.

8.5.1.1 Switching between the internal 10 MHz reference (X01, a temperature compensated crystal oscillator) and external 1 MHz, 5 MHz, or 10 MHz signals is provided by the EXTERNAL/INTERNAL reference switch on the rear panel of the 2500 and IC108, IC110, IC111, and their associated circuitry. The internal signal is always present at pin 12 of IC108. When the reference select switch on the rear panel is placed in the INT position, +5 volts is applied to pin 13 of inverter IC110. The output at pin 11 of IC110 goes from high to low, producing a high at pin 8 of IC108 and pin 13 of IC108. The high at pin 13 allows the 10 MHz internal reference at pin 12 to pass through, inverted, to pin 11. The low at pin 11 of IC110 is also applied to pin 5 of IC108, holding IC108 pins 6 and 1 high. When pin 1 of IC108 is high the oscillator signal at pin 2 is gated through, inverted, to pin 3 into the divider network of IC101 (pin 1). When the rear panel reference switch is in the INT position, the 10 MHz internal reference is gated through the two sections of IC108 to pin 1 of IC101, as described above. The reference is inverted in each section of IC108.

Note that the internal reference also passes through a buffer network in IC142 and resistors R160 and R170 to J105, the internal standard output jack on the rear panel. The resistors provide 50Ω output impedance for the signal. IC136 and its associated circuitry form a +5 volt regulator for X01, the reference oscillator.

8.5.1.2 An external standard (1 MHz, 5 MHz, or 10 MHz) is applied at J104 on the rear panel. Diode clippers CR102 and CR103, capacitors C109 and C110, and resistors R105 and R106 provide a 50Ω input impedance network. Comparator IC104 and its associated circuitry convert the input into a TTL signal at pin 9 which is applied to pin 2 of

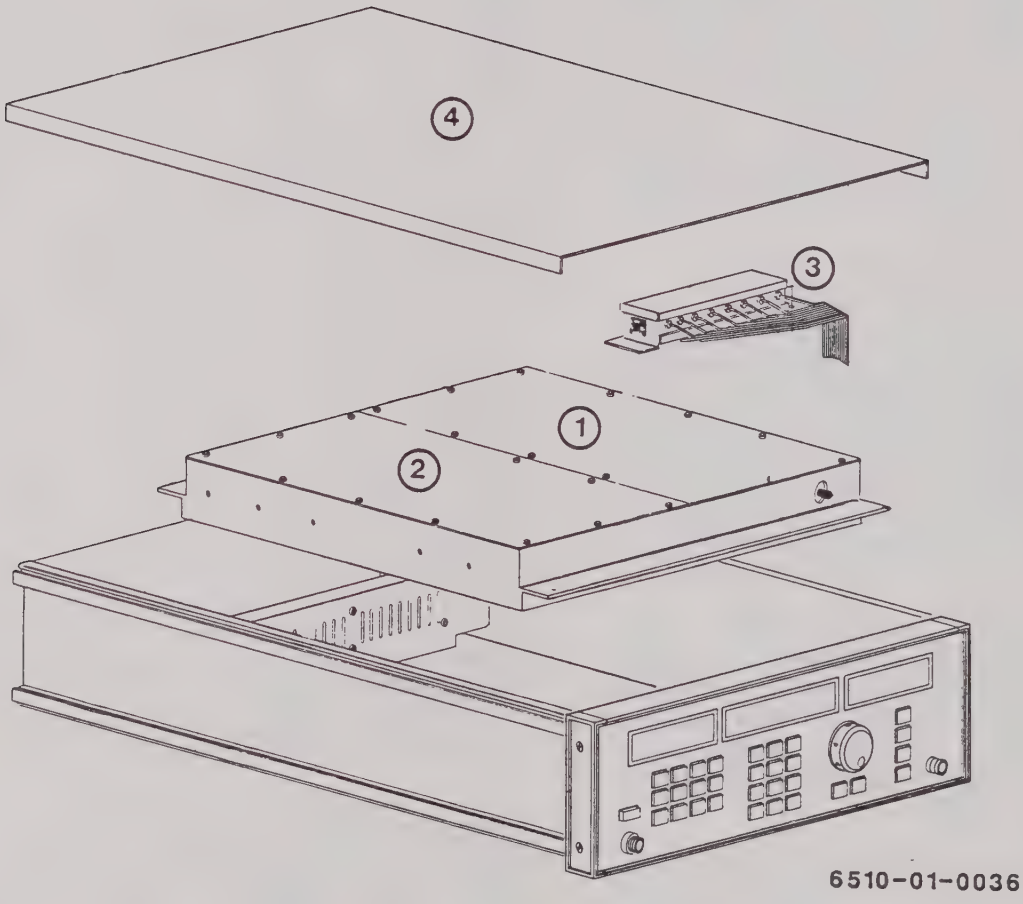


Figure 8-2. Top View, 2500

Key: 1. Oscillator Assembly
2. Amplifier Assembly
3. Attenuator Assembly
4. Top Cover

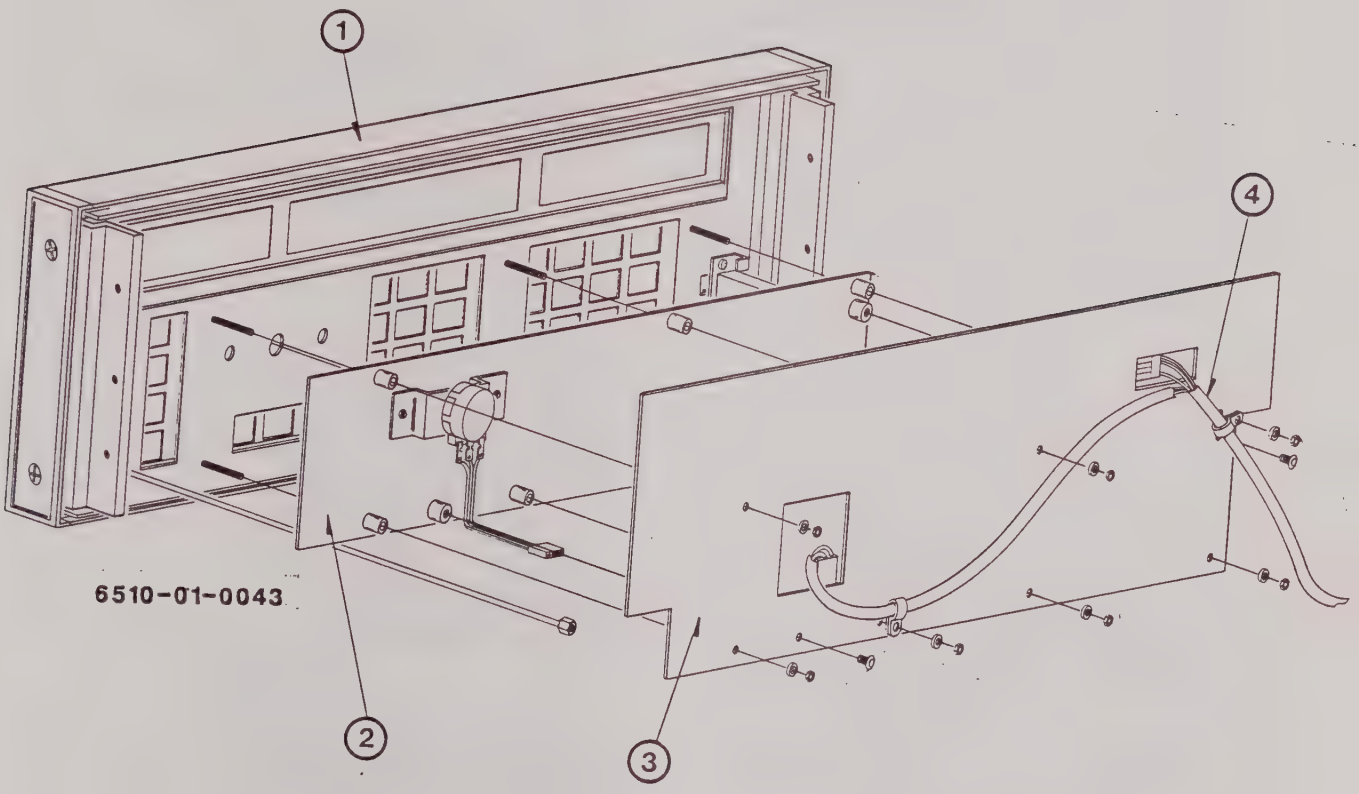


Figure 8-3. Front Panel Key/Display Board Relationship

Key: 1. Front Panel
2. Keyboard
3. Display Board
4. Backlight Cable

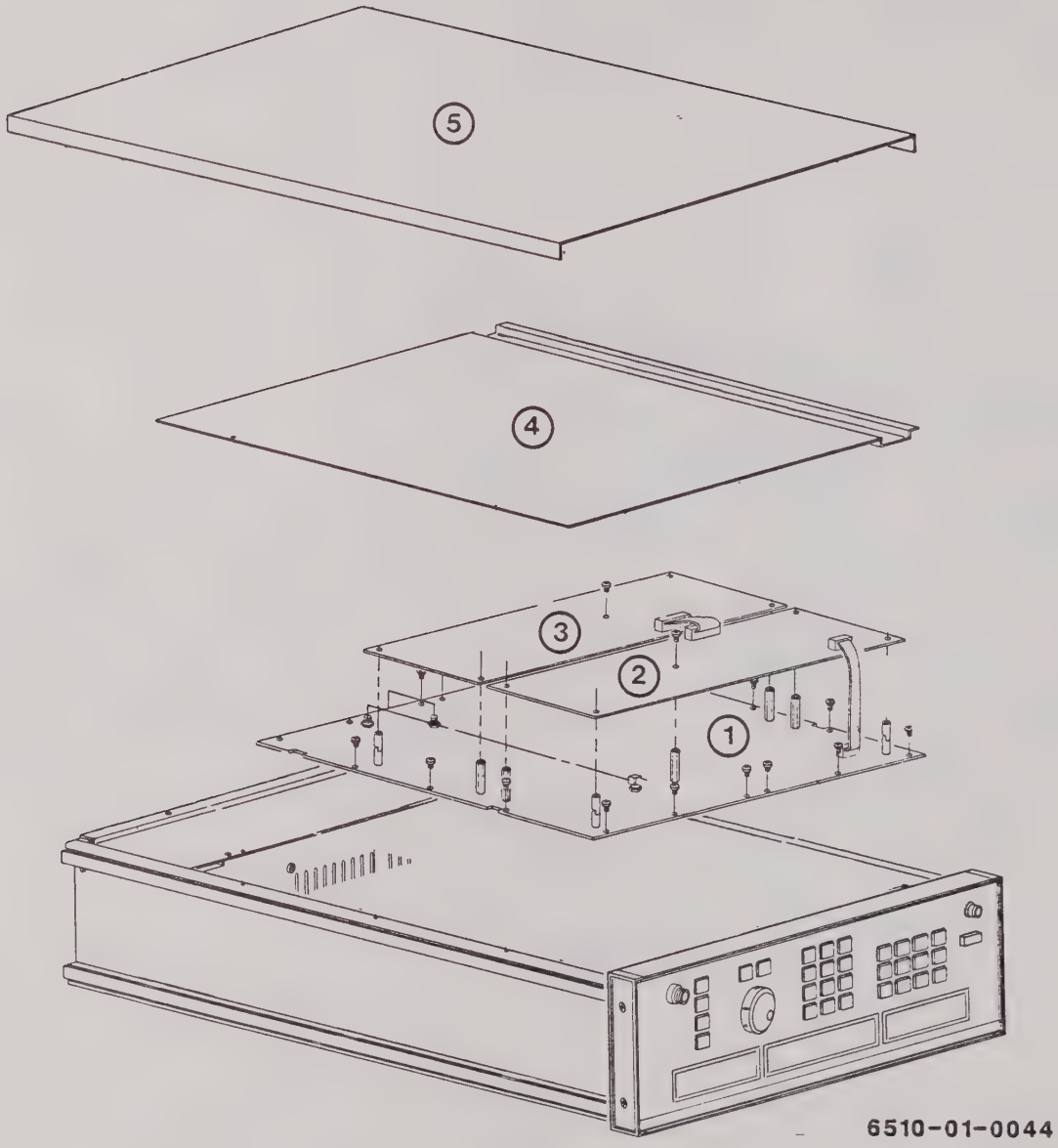


Figure 8-4. Bottom View, 2500

Key: 1. Main Board
2. Microprocessor Board
3. GPIB Board
4. Bottom Shield
5. Bottom Cover

IC110, buffered, and applied at pins 13, 5, and 9 of IC111. The particular gate selected is determined by the position of the reference select switch on the rear panel of the 2500. The reference select switch supplies only one 5 volt signal; the other positions on the switch are held low. If the switch is placed in the EXT 10 MHz position, +5 volts is applied through pin 2 of P102 to pin 2 of IC111.

Pins 1, 4, and 10 of IC111 are held high anytime the reference switch is not in the INT position because they are tied to pin 11 of IC111. (The low at pin 6 of P102 when the switch is not in the INT position produces a high at pin 11 of IC110.)

When pins 2 and 1 of IC111 are high, the input at pin 13 is gated through to pin 12 and applied at pin 4 of IC108. Pin 5 of IC108 is held high because it is tied to pin 11 of IC110 (see immediately above), therefore the 10 MHz, signal at pin 4 of IC108 is passed through to pin 6 to pin 1 and then to pin 3 of IC108 (because pin 2 of IC108 is tied to pin 11, which is high when the reference select switch is not in the INT position). The EXT 10 MHz signal is then applied to pin 1 of divider network IC101.

8.5.1.3 External 5 MHz and 1 MHz signals are selected in basically the same manner. Placing the reference select switch in the EXT 5 MHz position places a high (+5 V) on pin 11 of IC111. With a high at pins 11 and 10, the 5 MHz signal at pin 9 is gated through to pin 8 and then applied through pins 4 and 6 of IC110 to pin 4 of the divider network in IC101. The 1 MHz external signal is applied through pins 5 and 6 of IC111 and pins 10 and 8 of IC110 to pin 15 of IC101. The 1 MHz signal at pin 8 of IC110 also is the 1 MHz reference for the DDS circuitry, Main Loop Oscillator Assembly circuitry, and Local Oscillator Loop Oscillator Assembly. The signal at pin 8 may be gated directly through pin 10 as the product of a 1 MHz external reference. The signal at pin 8 may be gated through pin 9 as the product of the 10 MHz internal or 10 MHz external reference or the 5 MHz external reference after processing by and output at pin 7 of the divider network of IC101 (see immediately below).

8.5.1.4 IC101, IC102, and IC103 are dual binary frequency counters that divide the 10 MHz or 5 MHz or 1 MHz input into IC101 down to provide 1 kHz and 400 Hz internal modulating signals and a 1 MHz reference to the DDS and Oscillator Assembly circuitry. IC101 takes whatever input it receives (10 MHz, internal or external at pin 1; 5 MHz external at pin 4; 1 MHz external at pin 15) and counts the signal down to a 100 kHz output at pin 9 and a 1 MHz output at pin 7 (as necessary). IC101 contains divide by 2 (÷ 2) and divide by 5 (÷ 5) circuits that are wired together to produce the required count down. A 10 MHz input, for example, will be divided by 2 to produce the 5 MHz output shown at pin 3 of IC101. This 5 MHz output will be reapplied through pins 5 and 6 of IC110 to pin 4 of IC101. The 5 MHz will divide by 5 to yield the 1 MHz output at pin 7 of IC101. The 1 MHz output will be reapplied through pins 9 and 8 of IC110 to pin 15 of IC101 (and also to the DDS and Oscillator Assembly circuitry). The 1 MHz at pin 15 of IC101 will be divided by 2 to produce the 500 kHz output signal shown at pin 13, reapplied to IC101 at pin 12. The 500 kHz signal will go through a divide by 5 network and output at pin 9 as the 100 kHz signal applied to pin 4 of IC102. IC102 divides the 100 kHz input into a 1 kHz output (modulation source) at pin 13 and a 20 kHz output at pin 7. The 20 kHz is fed to pin 4 of IC103 and counted down to provide the 400 Hz modulation output at pin 13. The 1 kHz and 400 Hz modulation signals at pin 13 of IC102 and IC103, respectively, are each a square wave with a 50% duty cycle.

8.5.1.5 IC109 contains gate circuitry to select which modulation source, if either, is enabled. The 1 kHz signal is normally present at pin 4 of IC109 but must receive a select (enable) at pin 5 to pass through to pin 6. The same enable signal (from IC122, pin 4, on the Mod/Carrier Level schematic; Figure 10-3) gates the signal from pin 1 to pin 3 of IC109. IC106 and its associated circuitry form a low pass filter and the output level adjustment for the 1 kHz signal, with R114 controlling output level. The 400 Hz signal is normally present at pin 13 of IC109. It is selected by an enabling signal at pin 12 of IC109 (from pin 5 of IC122; Mod/Carrier Level schematic 10-3) and gated through to pin 11 and from pins 10 to 8 as described above. IC107 and associated circuitry provide a low pass filter and output level adjustment for the 400 Hz signal, with R115 controlling the output level.

The selected output, 1 kHz or 400 Hz, is applied to pin 2 of IC141, buffered, and fed from pin 6 of IC141 as output E to the Mod/Carrier Level circuitry shown on Figure 10-3 (see Section 8.5.2) where it provides the reference voltage for the Internal Modulation circuitry shown (on Figure 10-3).

The 400 Hz signal from pin 13 of IC103 also is fed as output A to the Mod/Carrier Level circuitry shown on Figure 10-3 where it provides a test signal fed back to the microprocessor to verify the 400 Hz circuitry (part of the power-up test procedure described in Section 5.5 of the Operating Manual).

8.5.1.6 An external modulation signal may be connected to J103. The signal will be applied to differential amplifier IC105 and sent as output D on the Mod/Carrier Level circuitry shown in Figure 10-3 for use as the voltage reference for the external modulation circuitry shown on Figure 10-3. Note that J103 has a floating ground.

8.5.1.7 IC137, IC138, and IC139 provide on-card regulation for the -18 V, +18 V, and +8 volt power sources, respectively, at P101.

8.5.2 MAIN BOARD, MOD/CARRIER LEVEL

The Main Board microprocessor interface to the carrier level and modulation control circuitry, the error interrupt requests, the carrier level and modulation control circuitry, and the reverse power protection circuitry are shown on the Mod/Carrier Level schematic (Figure 10-3).

8.5.2.1 IC113, IC114, and IC115 and their associated components form the microprocessor interface to modulation and carrier level control circuitry. Decoder IC113 processes the clock signals (clock, clock selects 0 - 2, and clock enable) from the microprocessor (P104, pins 9, and 1 - 4, respectively) to generate control clocks 0 - 4, the output at pin 10 (Y4), and the strobe signal to the various shift registers shown on the schematic. Control data from the microprocessor (P104, pin 8) is fed simultaneously to each of the shift registers (IC114, IC118, IC119, IC121, IC122, IC124, IC125, and IC127) and clocked bit by bit into a particular register(s) at each pulse of the appropriate clock. The serial data input is transferred into parallel data at the shift register outputs and is latched by the strobe signal.

8.5.2.2 IC115 is an 8 input Nor gate that receives error signals from the Oscillator Assembly circuitry (Main Loop Unlock, LO Loop Unlock, Over Deviation; J101) and Amplifier Assembly (Unlevel; J102) as shown and generates an interrupt request ($\overline{\text{FDB IRQ}}$) to the microprocessor if an error occurs. The output at pin 13 of IC115 is high (logic 1) during normal operation. Input lines to IC115 are low (logic 0). A +5 volt error signal input causes the output ($\overline{\text{FDB IRQ}}$) to go low. Error

signals are discussed in the Oscillator Assembly theory of operation (Sections 8.5.7 and 8.5.8). Error signals are also stored in shift register IC114 so that the microprocessor can interrogate the register to determine exactly which error generated the interrupt request (FDB Data line; pin 3 of IC114 to pin 5 of P104). The 400 Hz test signal input A from the Mod Source/Ref Freq circuitry (Figure 10-2) to pin 1 of IC114 (on Figure 10-3) provides a test signal that also is fed back to the microprocessor (to verify the 400 Hz circuitry as part of the power-up test procedure described in Section 5.5 of the Operating Manual).

8.5.2.3 The carrier level reference voltage is provided by IC116, a +10 volt reference. This DC level reference is applied to pin 6 of summing amplifier IC132. The AM signal used to amplitude modulate the carrier comes from pin 7 (internal AM) or pin 2 (external AM) of IC130 and is also applied to pin 6 of IC132. The summed reference voltage output at pin 7 of IC132 is applied to pin 15 of carrier level control DAC IC117. Carrier level control data (a 10 bit control word) from the microprocessor is clocked into and strobed through shift registers IC118 and IC119 onto pins 4 - 13 of DAC IC117. The reference input at pin 15 is multiplied by the control word to generate the required carrier level output from the DAC. Note that because the AM signal is mixed with the DC level reference at pin 6 of the summing amplifier (IC132) before both reference level components are sent to the control DAC, the AM component is automatically decreased or increased proportionally to any DC level change required to convert the reference voltage input at DAC pin 15 (of IC117) to the appropriate output level at pin 1 of IC132.

The carrier level output voltage at pin 1 of IC132 provides feedback to the DAC and is applied to AM level drive output buffer IC140. The AM drive signal is sent to the Amplifier Assembly through J102, pin 3. The return at pin 4 of J102 ensures that the AM/Level drive signal has the same ground reference on the Main Board and Amplifier Assembly.

8.5.2.4 The instrument RF output level is the product of the carrier level/AM drive output at pin 3 of J102 (as described above) and the programmable attenuator controlled by the outputs at pins 3-6 of shift register IC119. These control outputs are sent to Attenuator Driver IC129, which provides +12 volt outputs (powered by regulator IC135) to the Attenuator pad network identified at P103. Attenuator pads are energized as required by the +12 volt signals from IC129. For example, inserting thirty dB of attenuation will result in +12 volt levels at pins 1 and 2 of P103. When the maximum attenuation of 130 dB is realized, pins 1 - 6 of P103 will each have 12 volts applied.

8.5.2.5 Reverse power protection is provided by comparator IC112, transistors Q101 and Q102, and their associated circuitry. The actuating signal (minimum value between 0.61 and 0.67 VDC) comes from the reverse power detector in the Programmable Attenuator (see Section 8.5.15) through P8 of P103 on to pin 2 of IC112. It is compared to the reference voltage at pin 3. When the voltage at pin 2 is greater than the reference voltage at pin 3 it trips the reverse power protection circuit. The output at pin 1 causes transistor Q101 to turn off. The collector of Q101 goes high (+5 V), applying a high (+5 V) to the base of transistor Q102. Q102 turns on. The +5 volt normally present on the collector of Q102 changes to a low (ground) which is applied to pin 1 of Attenuator Driver IC129. The driver circuit normally converts the +5 volt input at pin 1 to a +12 volt output to the attenuator. When the +5 volt input at pin 1 goes low, so does the +12 volt signal at pin 18. The RF breaker (relay) in the Programmable Attenuator is held on by

the +12 volt signal at pin 7 of P103. When the 12 volt signal is removed, the breaker trips, removing RF power.

8.5.2.6 Shift registers IC121 and IC122, DAC IC120 and 1/2 of Dual Op Amp IC133 comprise the Internal Modulation select and fine tune circuitry shown on the Mod/Carrier Level schematic (Figure 10-3). The shift registers provide control data to the DAC and provide enable signals to select either the 1 kHz or 400 Hz internal modulation source. The outputs from pins 4 and 5 of shift register IC122 enable the 1 kHz and 400 Hz internal modulation sources, respectively, shown on the Mod Source/Ref Freq schematic (Figure 10-2; see text Section 8.5.1.5). Enables are positive logic, with a logic 1 (5 volts) providing the select signal. The truth table is shown in Table 8-1.

TABLE 8-1.
INTERNAL MODULATION SOURCE
SELECT TRUTH TABLE

	1 kHz Select	400 Hz Select	CW
IC122, pin 4	1	0	0
IC122, pin 5	0	1	0

External modulation and internal modulation can be applied simultaneously (complex modulation). When the unit is in the CW mode or when only external modulation is applied, neither internal source is enabled. The selected 400/1000 Hz internal modulation source input (signal E) from the Mod Source/Ref Freq circuitry (Figure 10-2) is applied to pin 15 of DAC IC120 (on Figure 10-3). This signal provides the reference voltage for the Internal Modulation circuitry. The internal modulation output at pin 7 of IC133 is applied to pin 16 of the DAC for a feedback reference and also to pin 6 of Quad Analog Switch IC130 and pin 11 of Quad Analog Switch IC131 for use as an internal AM or internal FM source. Switches IC130 and IC131 are controlled by software through shift registers IC122 and IC125. Action of these switches is described in detail in Section 8.5.2.8.

8.5.2.7 Shift registers IC124 and IC125, DAC IC123, and 1/2 of Dual Op Amp IC133 comprise the External Modulation select and fine tuning circuitry shown on the Mod/Carrier Level schematic (Figure 10-3). These shift registers provide control data to the DAC. Outputs from shift register IC125 also control the Analog Switches IC130 and IC131 used to route AM and FM signals to their proper destinations. The external modulation source (signal D from the Mod Source/Ref Freq circuitry; Figure 10-2) is applied to pin 15 of DAC IC123 (Figure 10-3). This input provides the voltage reference for the external modulation circuitry. The external modulation output at pin 1 of IC133 is fed to pin 16 of the DAC for a feedback reference and also to pin 3 of Quad Analog Switch IC130 and pin 6 of Quad Analog Switch IC131 for use as an external AM or external FM source.

8.5.2.8 Quad Analog Switches IC130 and IC131 are controlled by software through shift registers IC122 and IC125. An internal AM signal at pin 6 of IC130 will be passed through to pin 7 if the control signal at pin 8 is low (to put the switch in the closed position). An external AM signal at pin 3 of IC130 requires that switch to be closed (low at pin 1) before the signal can pass through to pin 2. The voltage at pin 1 opens or closes the switch. The control voltages at pins 8 and 1 come from pins 4 and 1, respectively, of shift register IC125. The selected AM signal (internal or external modulation) is applied to pin 6 of IC132 as described in Section 8.5.2.3, earlier. When no AM signal should be present (AM off), a low at pin 9 of IC130 closes the switch from pin 10 to

pin 11 and any incidental AM present is shorted to ground through the switch.

FM signals are routed through the switch from pin 11 to pin 10 (Internal Modulation) or the switch from pin 6 to pin 7 (External Modulation) of Quad Analog Switch IC131. Control voltages applied to pins 9 and 8 of these switches come from pins 3 and 15, respectively, of shift register IC125. When no FM should be present (FM off) pin 1 of IC131 closes the switch from pin 2 to pin 3 and any incidental FM present is shorted to ground through the switch.

Table 8-2 shows the truth table for switches IC130 and IC131 in complement-negative logic. A logic "1" indicates a low signal (0 volts) and a closed switch. A logic "0" indicates a high (+5 volts) and an open switch. An "x" indicates a "don't care" condition.

Note: FM and AM may be present simultaneously (complex modulation).

8.5.2.9 FM deviation is controlled (set) by software applied to the internal or external modulation DACs IC120 and IC123 through shift register pairs IC121/122 or IC124/125, respectively. These are 10 bit DACs. FM characteristics are specified in Section 1.2.7.2 of the Operating Manual for the Model 2500. A 10 bit DAC cannot provide the deviation resolution specified, therefore the Model 2500 incorporates two range multipliers (attenuators) of 20 and 40 dB. The multipliers are selected by shift register IC122, pins 2 and 3, and divide deviation into three ranges (with 2^{10} increments in each provided by the DACs). The deviation ranges are:

Range 1: 0 - 9.99 kHz;
10 Hz increments

Range 2: 10 kHz - 99.9 kHz;
100 Hz increments

Range 3: 100 kHz - 1 MHz;
1 kHz increments

TABLE 8-2.
MODULATION MODE SELECT TRUTH TABLE

	FM OFF	EXT FM	INT FM	AM OFF	EXT AM	INT AM	MOD OFF
IC130 pin 1	x	0	x	0	1	0	0
8	x	x	0	0	0	1	0
9	x	x	x	1	0	0	1
16*	0	x	x	x	x	x	0
IC131 pin 1	1	0	0	x	x	x	1
8	0	1	0	x	0	x	0
9	0	0	1	x	x	0	0
16	0	x	x	x	x	x	0

* Pins 16 of IC130 and 16 of IC131 are associated with the FM deviation range (see Section 8.5.2.9).

Resistors R157 and R148 are switched into or out of the FM signal path by control voltages at pins 16 of IC130 and IC131, respectively, to provide the three ranges of deviation. When a logic "1" is present at both pin 16 connections (complement-negative logic, therefore a "1" is a low voltage) both switches are open and the FM signal must go through both resistors. Maximum resistance is in the signal path. When pin 16 of IC130 receives a logic "1" while pin 16 of IC131 has a logic "0" (a high, closing the switch and shorting the signal around R148), the 10 kHz - 99.9 kHz range is selected. When both control pins are high, both switches are closed and the FM signal encounters minimum resistance (both resistors are effectively shorted out). The 100 kHz - 1 MHz deviation range is selected. The FM deviation range truth table is shown in Table 8-3.

TABLE 8-3.
DEVIATION RANGE SELECT TRUTH TABLE

	Deviation Range, ± kHz		
	0-9.99	10-99.9	100-1000
IC122, pin 2	1*	1	0
pin 3	1	0	0

* Negative Logic

8.5.2.10 FM Deviation Correction DAC IC126, one half of dual op amp IC134, and shift register IC127 comprise the Deviation Correction circuitry shown on the Mod/Carrier Level schematic (Figure 10-3). The Oscillator Assembly VCO gain (see Sections 8.5.7 and 8.5.8 for greater detail) varies as a function of its frequency. FM deviation varies with VCO gain. The FM signal at pin 1 of IC134 is applied to pin 15 of the Deviation Correction DAC IC126. It is multiplied by a deviation correction factor (pins 4-11) provided by software through shift register IC127. The correction factor is derived from the frequency AutoCal® routine. The coarse tune values stored during the AutoCal® routine comprise the VCO tuning curve, the derivative of which is the VCO gain curve. The inverse of the gain curve essentially programs the Deviation Correction DAC (provides the correction factor as a function of VCO frequency). The process described above produces an output from pin 7 of IC134 in the Deviation Correction circuitry that has an acceptably flat frequency deviation response with changes in VCO frequency. This output is sent to the VCO through pin 3 of J101.

8.5.2.11 The FM enable to the Oscillator Assembly (pin 1 of J101) is controlled by pin 2 of shift register IC119.

8.5.2.12 Note that when all modulation is turned off, the Modulation DACs (IC120, IC123, and IC126) are programmed for minimum outputs.

8.5.3 MAIN BOARD, FREQ DIV/CONTROL

The Main Board Freq Div/Control schematic (Figure 10-4) shows the Single Side Band (SSB) Mixer, Main Loop Fractional Frequency Divider and its Fraction Control Section, the pulse stretcher network, the Local Oscillator Divider (÷ 500), and the shift registers associated with Oscillator and Amplifier Assembly Control signals.

Figure 8-5 shows the Main Phase Locked Loop (PLL) in block diagram form. The SSB and Main PLL divider circuits are detailed in Figure 10-4. The Direct Digital Synthesis (DDS) circuitry is shown in Figure 10-5. The remaining blocks in Figure 8-5 are described with the Oscillator Assembly (Sections 8.5.7 and 8.5.8).

8.5.3.1 The Single Side Band (SSB) Mixer MX401 (see Figure 10-4) receives input signals from the Oscillator Assembly (from J401 to pin 16 of the SSB

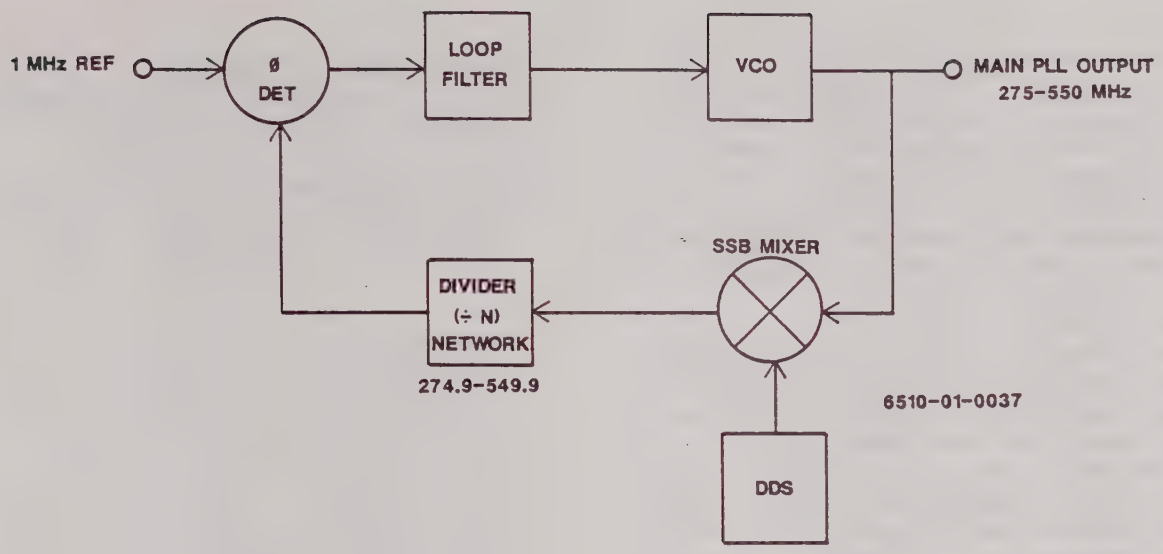


Figure 8-5. Block Diagram, VCO Main Phase Locked Loop (PLL)

mixer) and the Direct Digital Synthesis (DDS) section (at pins 4 and 13 of the SSB mixer). The 275 - 550 MHz fundamental band signal (f_o) from the Oscillator Assembly is mixed with the two identical frequency (but 90° out of phase) 100 - 199.999 kHz signals (f_{DDS}) from the DDS section. Mixed frequency signals (f_{mix}) that are the sum and difference of the two input signals are produced. The relationship is:

$$f_{mix} = f_o \pm f_{DDS}$$

Conversion loss for the lower sideband (the difference of the frequencies) is about 9 dB. Upper sideband (the sum of the frequencies) rejection is an additional 15 dB from the lower sideband. In effect, the lower sideband is passed through to the Main Loop Frequency Divider (from pin 1 of the SSB mixer) while the upper sideband is eliminated. For example, if f_o = 300 MHz and f_{DDS} = 100 kHz,

f_{mix} = 300 MHz ± 100 kHz
f_{mix} = 300 MHz + 100 kHz = 300.1 MHz
and 300 MHz - 100 kHz = 299.9 MHz
f_{mix} = 300.1 MHz and 299.9 MHz

The upper sideband (300.1 MHz) is eliminated. The lower sideband (299.9 MHz) will be sent to the Main Loop Fractional Frequency Divider (described below).

8.5.3.2 The Main Loop Fractional Frequency Divider is a high speed ECL synchronous fractional frequency divider. It is composed of dual modulus (÷ 10/11) counter IC401, modulus control binary counter IC402, decade counters IC403 and IC404, ECL to TTL translators Q401 and Q402, a fraction control section (described below), and associated circuit components. It is programmed to divide the input at pin 16 of IC401 by values between 274.9 and 549.9 in 0.1 steps. (Pin 15 of IC401 provides a bias reference voltage to pin 16).

The lower sideband output from SSB mixer MX401 is amplified by 10 dB gain RF amplifier IC426 and then applied to the input of the main loop divider (pin 16 of IC401). Counters IC401 - IC404 each control one decade of MHz down counting. IC404 processes the 100's MHz decade. IC403 processes the

10's MHz decade. IC402 controls the 1's MHz decade. IC401 is part of the fraction control section that controls the 1/10's MHz decade. The counters count upward from a preset starting count value. The 100's, 10's, and 1/10's counters are preset in 9's complement logic. The 1's position is preset in 2's complement logic.

8.5.3.3 The fraction control section of the Main Loop Divider consists of decade counters IC405 and IC406, adder IC409, quad NAND gates IC419 and IC420, shift register IC410, and their associated circuit components. The fraction control circuit causes the integer part of the divider network (IC402 - IC404) to toggle between two integer values over a 10 µsecond period, after which the two partial counts are summed to effectively generate an average division value that is somewhere between the two integers used. For example, if the input to the divider were 319.7 MHz, the divider must divide by 319.7 MHz to generate the 1 MHz output to the Oscillator Assembly at pin 12 of J101 (to lock the Main Loop as required). To divide by 319.7 MHz, the divider will divide by 319 for part of the division cycle and by 320 for the remaining part of the division cycle. A division cycle is broken into 10 frames of 1 µsec each. The 1 µsec clock that controls the fraction control section comes from the collector of transistor Q401 (part of the ECL to TTL translator circuitry). For a count rate n = 319, 319 pulses will be counted per pulse out per frame. For n + 1 = 319 + 1 = 320, 320 pulses will be counted per pulse out per frame. Because 319.7 is 7/10 of the way between 319 and 320, the divider will be programmed to divide by 320 for seven of the ten frames in a division cycle and programmed to divide by 319 for the remaining three frames.

The average division per frame over the entire division cycle will be the sum of input pulses divided by 320 and by 319 over the entire cycle divided by the number of frames per cycle.

The actual division sequence will be:

Frame #	Divide by
1	320
2	320
3	320
4	320
5	320
6	320
7	320
8	319
9	319
10	319

Total pulses in are 320 times 7 frames = 2240 pulses plus 319 times 3 frames = 957 pulses. Total pulses in are 2240 plus 957 = 3197 pulses. The average division per frame is 3197 ÷ 10 = 319.7 pulses, for an average network division rate of 319.7.

Shift registers IC410 and IC411 provide control information from software (the microprocessor) to counters IC403 - IC406 and adder IC409. The adder determines whether division during a frame is by the "n" or "n+1" value by adding a "0" or a "1" to the 1's decade of the division number before it is sent to counter IC402. Register networks IC407 and IC408 convert the TTL signals from IC409 - IC411 into the ECL levels appropriate for counters IC402 - IC404.

The 100 kHz data lines from IC410 (pins 3 - 7) program decade counter IC406 to count at the "n+1" rate for the first part (number of frames) in the division cycle, then count at the "n" rate for the remaining frames. The output at pin 3 of NAND gate IC421 determines whether adder IC409 adds a "0" or a "1" to the 1's MHz decade (to vary the 1's decade of the integer count number). The line (to pin 6 of IC409) will be

high during the parts of a division cycle when division is by the "n+1" value (the adder adds a "1" to the "n" value). Counter IC406 will take the line low when counting is to be done at the "n" count rate. Counter IC405 keeps track of frame count to establish each division cycle and provides the $\overline{\text{LOAD}}$ signal to IC406 (pin 9).

8.5.3.4 The Main Loop Fractional Frequency Divider output at the collector of Q401 is applied to pin 13 of IC421 as 1 µsec pulses of approximately 50 nsec duration. IC423 is a one shot flip-flop (monostable multivibrator) that acts as a pulse stretcher, converting the 50 nsec input pulses into approximately 200 nsec pulses (150 - 200 nsec) at pin 8 of IC421.

8.5.3.5 The Local Oscillator Divider is composed of prescaler/counters IC415 - IC417 and their associated circuitry. The 500 MHz drive input from the Oscillator Assembly (J402) is applied at pins 15/16 of prescaler IC415. The prescaler is a divide by 10 or 11 only counter that is set to divide by 10. The 500 MHz input is counted down to a 50 MHz output at pin 11 of the prescaler. The 50 MHz goes through a divide by 10 counter (IC416) which provides a 5 MHz output at pin 11. The 5 MHz signal is fed through one of the NAND gates of IC420 (output at pin 11) into divide by 5 counter IC417. The 1 MHz output at pin 7 is fed through pin 18 of J101 to the phase detector in the Oscillator Assembly Local Oscillator Loop to lock the loop at 500 MHz. (See Section 8.5.8 for greater Oscillator Assembly detail.)

8.5.3.6 Shift registers IC412, IC413, and IC414 process Oscillator Assembly Coarse Tune Control and Bandswitching data and the Local Oscillator Enable signals shown at J101 and also the Amplifier Assembly signals shown at J102. These signals are described in the Oscillator and the Amplifier Assemblies text, respectively.

8.5.4 MAIN BOARD, DIRECT DIGITAL SYNTHESIS

The Direct Digital Synthesis (DDS) circuitry shown in Figures 8-5 and 11-5 controls the 10 kHz, 1 kHz, 100 Hz, and 10 Hz digits in the fundamental frequency (275 - 550 MHz) band. For a fundamental frequency of 325.41652 MHz, for example, the 325.4 digits are controlled by the Main Loop Divider (see Section 8.5.3.2) and the last four digits (1652) are determined by the DDS circuitry. (When the 2500 output is 550 MHz or greater, software programs the DDS signal in 5 Hz steps so that the 10 Hz instrument resolution is maintained when the Main Loop Output is doubled to generate an RF output of 550 MHz or greater. Refer to the text description of Frequency Conversion, Section 8.5.10).

8.5.4.1 Figure 8-6 is a block diagram of the DDS circuit. The output from the DDS circuit is generated from the look up sine table in EPROM IC212 as it is accessed by the Phase Accumulator Network. The 64K (8K x 8) bit EPROM contains 2000 addresses with eight-bit binary numbers which represent the voltage levels at 0.18 degrees of phase angle along a sine wave (see Figure 8-7). Each address in sequence from 0000 to 1999 contains the voltage representation associated with that point on the sine curve. The eight bit binary numbers represent 2^8 or 256 different voltage levels.

8.5.4.2 The phase accumulator network includes the shift registers (IC201, IC202, and IC203), BCD Adders (IC204, IC205, IC206, IC207, and IC208), Octal D type flip-flops (IC209, IC210, and IC211) and two of the gates in IC220. The output from the phase accumulator network provides the EPROM address from which the 8-bit binary voltage representation is taken (address lines A_0 - A_{11} on IC212). The EPROM address "n" is incremented some number "k" (the phase increment input from

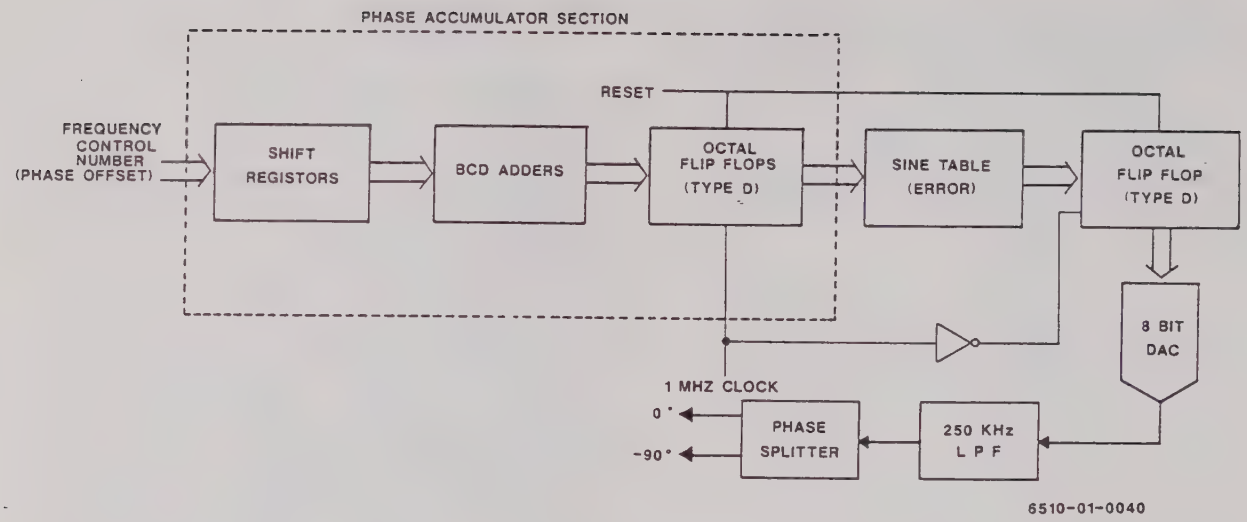


Figure 8-6. DDS Circuit Block Diagram

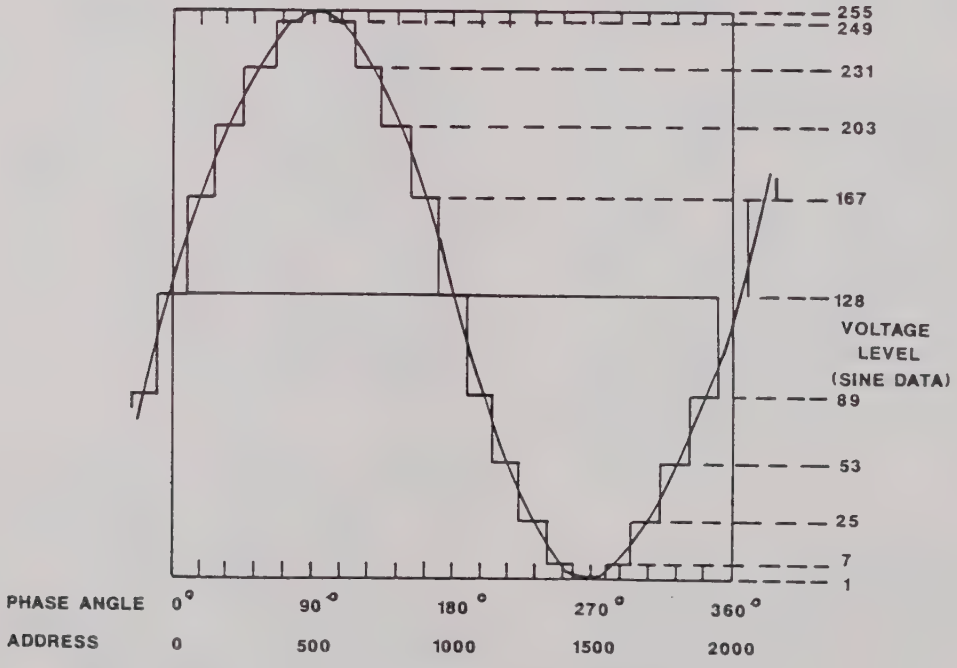


Figure 8-7. Sine Wave Phase Angle/Address/Level Representation

software) at each clock pulse to generate (synthesize) the required output frequency. The pulse from inverter IC220, pin 3 clocks the octal flip-flops to latch the address (which is the new accumulator value). For example, if k = 1, then at each clock pulse the look-up address "n" is incremented by 1. The phase accumulator network is reset to n = 0 any time frequency is changed; therefore the first frequency control number (see Figure 8-6) clocked through the shift registers to the adder series and into the sine table EPROM is n = 0. At the next clock pulse the address is incremented k = 1 to address n = 1. At the next clock pulse the address n = 1 is incremented by k = 1 and becomes n = 2. Flip-flops IC209 - IC211 provide feedback as shown to the series of adders. The sequence of address increments with k = 1 is shown below:

for k = 1

0000 first address n_1 = 0 (reset)
0001 $n_2 = n_1+k = 0+1 = 1$
0002 $n_3 = n_2+k = 1 + 1 = 2$
0003 $n_4 = n_3+k = 2 + 1 = 3$
.
.
.
0999
1000
1001
.
.
.
1998
1999
0000 rolls over to 0000 again

When k = 1, each address of the look-up table EPROM is accessed at a rate of 1 address per clock cycle (1 µsec). It requires 2000 µsec to get one cycle out at this address increment (frequency control) number. The output frequency at k = 1 is therefore

$$f_o = \frac{1}{2000\ \mu sec} = 500\ Hz$$

Consider the case when k = 5. The phase accumulator is reset to n = 0 but each successive increment (k = 5) increases the phase angle of the output by .9° (.18° x 5) skipping to every 5th address (rather than every address as when k = 1). The address sequence will be:

for k = 5

0000 first address n_1 = 0 (reset)
0005 $n_2 = n_1+k = 0 + 5 = 5$
0010 $n_3 = n_2+k = 5 + 5 = 10$
0003 $n_4 = n_3+k = 10 + 5 = 15$
.
.
.
0995
1000
1005
.
.
.
1990
1995
0000 rolls over to 0000.

When k = 5 the complete look-up table is accessed five times as rapidly as when k = 1 because every 5th address is accessed at each clock pulse. It requires 400 clock pulses (1 µsec/pulse) to generate one cycle out. Therefore the output frequency at k = 5 is

$$f_o = \frac{1}{400\ \mu sec} = 2500\ Hz$$

The general equation for output frequency (f_o) as a function of phase offset (k) is:

$$f_o = f_{clk} \times \frac{k}{n_{full\ scale}}$$

where f_{clk} = the frequency of the clock = $1x10^6$ Hz and $n_{full\ scale}$ is 2000 or the maximum number of EPROM addresses available.

Note that this equation expresses output frequency as a function of the rate

at which one complete cycle is synthesized from the look-up table EPROM. That rate is a function of the address increment steps k, used to step through the table.

8.5.4.3 The 1 MHz reference for the DDS circuit provides clock pulses at 1 μsec intervals.

8.5.4.4 The phase accumulator section processes the phase increment input (frequency control number) from software (pin 14 of IC201) to increment the series of BCD Adders the required number k. BCD Adder IC208 processes the least significant digit of the frequency control number (phase increment input). Adder IC207 processes the next least significant digit. Adders IC208 and IC207 do not address the EPROM, therefore these two adders allow k to be a fractional value as low as 0000.01, permitting an output frequency resolution of 5 Hz. For k = 0.01, for example, output frequency (f_o) is:

$$f_o = f_{clk} \times \frac{k}{n_{full\ scale}}$$

$$f_o = 1x10_6 \text{ Hz} \times \frac{.01}{2000}$$

$$f_o = 5 \text{ Hz}$$

when the hundreds digit controlled by IC208 is full, the carry (pin 6 of IC208) steps IC207 up one unit (one tenth). When the tenths digit controlled by IC207 is full, the carry (pin 6 of IC207) is fed to IC206 (pin 5) to step the ones place up one unit.

8.5.4.5 In summary, at each clock pulse the phase accumulator network provides an address that is latched through octal flip-flops into the sine table EPROM. The address is incremented some value k (the phase increment input; the frequency control number) at each clock pulse. This number k is basically the number of degrees along the sine curve that the address n is incremented at each clock pulse.

8.5.4.6 The output from the EPROM at each clock pulse is an 8 bit binary number representative of the sine wave voltage at the associated sine wave phase angle. This number is latched by flip-flop IC213 into 8-bit DAC IC214. The pulse from pin 8 of inverter IC220 clocks the 8-bit binary word through IC213 into the DAC (IC214).

8.5.4.7 DAC IC214 converts the input binary word into the equivalent output current at pin 4. The output is fed to pin 2 of low noise amplifier IC215. IC221, a 10 volt reference, provides an offset to low noise amplifier IC215.

8.5.4.8 The output at pin 6 of IC215 is applied through the 2 stage low pass filter comprised of IC216 and IC217 and associated circuitry. The cutoff for the low pass filter is 250 kHz.

8.5.4.9 The filtered signal at pin 6 of IC217 is sent to the phase splitter network of IC218, IC219, and associated circuitry. The outputs at pins 1 and 7 of IC219 are identical in voltage level and frequency but 90° out of phase with one another.

8.5.5 POWER SUPPLY

The Model 2500 Power Supply (see Figure 10-6) provides the DC power for the instrument circuitry and fan and also provides the AC power used for backlighting the front panel displays.

8.5.5.1 AC input power passes through the line filter (shown inside the dashed lines between rear panel AC receptacle J1006 and Jack J1005) and then through either a 1 amp or 0.5 amp fuse (F1002), depending upon the input voltage source. Input power is then routed through power switch S1001 and to the primary of transformer T1001.

8.5.5.2 The instrument will operate from a 100 VAC, 120 VAC, 220 VAC, or 240 VAC source. The voltage selection wheel in the rear panel AC power con-

nector module (see Figure 2-1 of the Operating Manual) must be rotated to show the proper input voltage through the small window in the module (the module's full cover must be removed to rotate the selector wheel).

8.5.5.2.1 The voltage selector wheel opens and closes the switches associated with the primary of T1001 as shown in the Line Voltage Selector table on the power supply schematic (Figure 10-6) to configure the transformer primary as required.

8.5.5.2.2 When a 120 VAC source is selected, for example, switches M, I, and J are closed, as shown in the table. Switches H and K are open. Each of the two primary windings are in parallel across the "voltage in" lines (at pins 3 and 4 of J1005).

8.5.5.2.3 When a 240 VAC source is selected the primary windings are configured in series.

8.5.5.3 The secondary of T1001 has five taps; the center tap is grounded.

8.5.5.4 CR1001 is a bridge rectifier providing full wave rectification of the signal across the secondary of T1001. Each half of the input cycle charges capacitor C1001 to provide a +27 VDC level at pin 1 of J1002 and at the collector of voltage regulator Q1002. Each half of the input cycle also charges C1008 to put a -27 VDC level at pin 6 of J1002 and at the emitter of voltage regulator Q1004.

8.5.5.5 The +18 VDC at pins 2 and 3 of J1002 is produced by +18 VDC regulator Q1002 which is controlled by its base voltage. Voltage reference IC1001 provides +5 VDC to pin 3 of operational amplifier IC1002A. When the +18 volt regulator (Q1002) is at +18 V, voltage divider network R1004, R1005, and R1008 feeds a +5 volt level back to pin 2 of IC1002A. If the voltage out from the regulator drops, the voltage output at pin 1 of IC1002A increases in response to the decrease in input signal at pin 2. The output at pin 1 of IC1002 is applied to the base of regulator Q1002. When base voltage increases, emitter voltage increases, and the +18 volt supply returns to +18 volts. Resistor R1005 is the +18 V adjust.

8.5.5.5.1 FET Q1001 is a current source, supplying current to R1006 to raise the control voltage to the base of Q1002 as needed.

8.5.5.5.2 Diode CR1003 provides protection for electrolytic capacitor C1003 (prevents a negative voltage at pins 2 and 3 being fed to the capacitor).

8.5.5.6 The -18 VDC at pins 4 and 5 of J1002 is produced by -18 V regulator Q1004 which is controlled by its base voltage. The output from pin 7 of op amp IC1002B controls transistor Q1003 which controls the -18 V regulator. Op amp IC1002B receives a ground (zero volt) reference input at pin 5. The voltage divider network R1009, R1010, and R1011 (from +18 V to -18 V) sets the other input (pin 6) to zero (0) volts when the -18 V (and +18 V) levels are accurate. R1010 is the -18 V adjust. If the -18 volt output goes lower (to -17 volts, for example), the input at pin 6 of IC1002B will go positive, forcing pin 7 negative. The negative will be applied to the base of Q1003 which will turn Q1003 on harder. When Q1003 conducts harder, more base current is drawn from regulator Q1004 and the output voltage goes back to -18 volts.

8.5.5.6.1 Diode CR1005 provides protection for electrolytic capacitor C1009, preventing a positive voltage at pins 4 and 5 being fed to the capacitor.

8.5.5.7 The voltages fed through diodes CR1006 and CR1007 to C1010 provide an unregulated +12 volts to Darlington power transistor Q1005. The

three diode voltage drop (approximately 0.6 volts per diode; two diodes in Q1005 and CR1011 the third) of 1.8 volts lowers the +12 volt input to a +10.2 volt level to the fan (J1003, pin 1). The +10.2 volts results in a longer operating life for the fan and quieter operation.

8.5.5.8 The +8 volt supply at pins 7 and 8 of J1002 is produced by +8 volt three terminal voltage regulator IC1003. The +12 volts input at terminal 3 is regulated to +8 volts at terminal 2 using output feedback through the resistor network and capacitor C1011. One or the other of resistors R1017 and R1019 is factory selected to trim the regulator output to +8 volts, if needed. (If R1016 and R1018 produce a +8 V output neither trimming resistor will be used).

8.5.5.8.1 Diode CR1008 protects the regulator from a negative input at pins 7 or 8.

8.5.5.9 The 125 VAC source at pin 3 of J1004 is used for display back-lighting. AC power supply module E1001 provides a 125 VAC low current source out when transistor Q1007 conducts. The collector of Q1007 receives 27 volts across filter network R1022, C1012, and R1023. Zener diode CR1009 supplies a +12 volt level to the base of Q1007 and the collector of transistor Q1006. When Q1006 conducts, Q1007 is turned off and the 125 VAC source is not present at pin 3 of J1004. The BACKLIGHT $\overline{\text{ENABLE}}$ signal at pin 1 of J1004 turns off Q1006 by shorting its base to ground. When Q1006 turns off, Q1007 conducts, supply 11.4 volts to pin 1 of E1001 and the output at pin 3 of EC1001 is 125 VAC. The frequency of the 125 VAC out is approximately 1.7 kHz and is determined by the internal circuitry of the AC power module. The 1.7 kHz output results in longer life for the electroluminescent (EL) displays.

8.5.5.10 The +20 VAC output shown at pin 9 of J1002 is not used in this unit.

8.5.6 MICROPROCESSOR BOARD

The Microprocessor Board (see Figure 10-7) contains a power up (reset) circuit, the microprocessor, a memory management section, a serial data decode section, and interrupt circuitry.

8.5.6.1 When power is first applied, transistors Q301 and Q302 and associated components ramp power up to prevent voltage spikes. A low on the $\overline{\text{reset}}$ line at the collector of Q302 is applied to pin 1 of the microprocessor (IC301) to initialize it and start program execution.

8.5.6.2 The eight bit microprocessor (IC301) has two I/O ports. Port A (PA0 - PA7; pins 14 - 7) provides serial communication to offboard circuits (system selects, the clock, data, etc). Port B (PB0 - PB7; pins 36 - 29) provides parallel GPIB communication. Lines B0 - B7 (pins 28 - 21) may carry address or data information. Lines A8 - A12 (pins 19 - 15) are address lines. Address and data strobe signals are at pins 6 and 4, respectively. The read/write (R/$\overline{\text{W}}$) output line is at pin 5. The interrupt request ($\overline{\text{IRQ}}$) input is at pin 2. The 4 MHz crystal (X301) input at pins 38, 39, and 20 (gnd) is counted down internally to produce the 1 MHz system clock.

8.5.6.3 The memory management section of the microprocessor board includes the decode chips (IC302, IC303, IC304), RAM (IC305), ROM (IC306 - IC308), and gate/inverter circuitry (IC309, IC315, IC317, IC321, IC323) shown across the top section of Figure 10-7.

8.5.6.3.1 Octal 3-state latch IC302 acts as a demultiplexer, converting 8-bit address/data information input from lines B0 to B7 of the micro-

processor into RAM/ROM address lines A0 - A7 (at 8Q to 1Q) and chip select signals to the gate and decode chips, as shown.

8.5.6.3.2 The top five address lines (A8 - A12) are fed to pins 2 - 5 of dual NOR gate IC315 and pin 9 of inverter IC323. The outputs at pins 1 and 8 of these chips, respectively, are sent to pins 13 and 1 of NAND gate IC321. They are added to the A7 output from IC302 to provide the select (enable) signal to pin 18 of RAM chip IC305 (from pin 12 of IC321).

8.5.6.3.3 The three ROM chips (IC306 - IC308) each have 8k bytes of memory organized as two banks (top/bottom) of memory. Each bank has 4k bytes of memory. Memory is apportioned as follows:

ROM	Top Bank	Bottom Bank
IC306	Core	Diagnostics
IC307	Display	Default
IC308	AutoCal®	RF Control

8.5.6.3.4 The Octal D type flip-flops in IC304 and NAND gates in IC321 act as a decoder to control bankswitching between the ROM memory banks. Decode logic to the NAND gates comes from Microprocessor address signals (line A8 - A12) sent through a NOR gate in IC315 (output at pin 13) and inverter IC323 (outputs at pins 2 and 4). The 1 of 8 decoder IC303 and its associated NAND gates (IC317) form a latch circuit to clock decoder IC304. (IC303 also plays an important role in the interrupt circuit; see Section 8.5.6.4).

8.5.6.3.5 The NAND gates in IC318 and IC319 provide the decode logic for serial communication and control/handshaking signals at I/O port A (PA0 - PA7) of the microprocessor (IC301). The serial data input to the microprocessor (RTN DATA) at pin 3 of IC319 is selected by the FP/$\overline{\text{MAIN}}$ line at PA4 and may represent front panel data (from pin 12 of J301) or FDB Data from the main board (from pin 5 of J305). The FP/$\overline{\text{MAIN}}$ signal also is processed through inverter IC323 (pins 5 to 6) and pins 2 and 5 of IC318 to select (enable) the FP (at pin 13 of J301) or the RF circuitry (at pin 4 of J305). Enabling the Front Panel disables the RF Main input and visa-versa.

8.5.6.3.6 The signals at PA0 and PA1 ($\overline{\text{GPREQ}}$ and $\overline{\text{GPACK}}$; pins 1 and 2, respectively, of J302) set the mode for GPIB operation. The SERIAL/$\overline{\text{GPIB}}$ line at PA3 of the microprocessor is the GPIB initialization signal ($\overline{\text{GPIB INT}}$ at pin 3 of J302). GPIB data communication between the microprocessor and the GPIB Board is through pins 7-14 of J302.

8.5.6.4 The interrupt circuitry consists of latch IC310, D-type flip-flops IC311 and IC312, the NAND gates in IC314, IC316 and IC320, the inverters in IC324, the buffer/line drivers of IC322, and the pull-up resistor network of IC312. Interrupt requests from the keyboard ($\overline{\text{KBD IRQ}}$; pin 11 of J301), the spin knob ($\overline{\text{KNOB IRQ}}$; pin 8 of J301), main board feedback ($\overline{\text{FDB IRQ}}$; pin 6 of J305) and the GPIB card ($\overline{\text{GPIB IRQ}}$: pin 6 of J302) are applied as lows to pins 1, 3, 5, and 9, respectively, of the inverters in IC324. Each inverter output (high) is applied two places simultaneously. The $\overline{\text{KBD IRQ}}$ high at pin 2 of IC314, for example, is applied to pin 2 of NAND gate IC316. Because pin 1 of IC316 is typically high (from latch output Q1 of IC310) the output of IC316 at pin 3 goes low which produces a high at NAND gate IC314 output pin 6. The high from pin 6 produces a low at pin 8 of IC314 which is the $\overline{\text{IRQ}}$ input to the microprocessor IC301. This signal will inform the microprocessor that one of the interrupts has been received and service is requested.

Note that Q1 - Q4 outputs from latch IC310 are programmed for logic 0 or 1 (low or high; 0 or +5 volts) by inputs B0 - B3 (pins 7, 6, 3, and 2, respectively) from the microprocessor. If

all four outputs are programmed high, their associated inputs to the NAND gates of IC316 (pins 1, 4, 10, and 13, respectively) are high and all four interrupts are enabled (any interrupt that goes low will be inverted by IC325 and will be fed through its associated gate in IC316 because the other input to the gate is programmed high from the Q1 - Q4 output of IC310). Programming any of the Q1 - Q4 outputs from IC310 low will automatically disable the associated interrupt because its associated NAND gate in IC316 will be turned off by the low from the Q1 - Q4 output.

The second place the $\overline{\text{KBD IRQ}}$ high at pin 2 of IC324 is sent is to the clock 1 (CK1) input of flip-flop IC311. The Q1 output of IC311 will go low and be applied to buffer/line driver IC322 at pin 2. The low will remain at pin 2 until another CK1 pulse is applied or the flip-flop is reset. The status of the signals at pins 2, 4, 6, and 8 of IC322 are read by the microprocessor as the lower 4 bits (B0 - B3) of the data/address lines. The interrupt request (IRQ) at pin 2 of the microprocessor will set the R/$\overline{\text{W}}$ and DS lines from pin 5 and 4, respectively, of the microprocessor and the enables from pins 9 and 10 of decoder IC303 so that these four signals (R/$\overline{\text{W}}$, DS, the two selects from IC303) are applied to the NAND gates in IC320 (the lower address decode logic) to enable IC322. With IC322 enabled, the microprocessor will read the status of pins 2, 4, 6, and 8 of IC322 through lines B0 - B3 and determine which interrupt request was received. In this example pin 2 would be read as low (logic 0). The microprocessor would perform those routines associated with a Keyboard Interrupt Request and when finished would send the required R/$\overline{\text{W}}$, DS, and two selects signals to IC320 to enable latch IC310 and reset IC311 (by dropping the Q1 (pin 16) output of IC310 low). The B3 - B0 inputs from the microprocessor at pins 2, 3, 6, and 7 of IC310 determine the Q1 - Q4 output status. Note that CR302 through CR305 are LEDs associated with the interrupt resets and turn on to indicate the interrupt being serviced. The association is as follows:

CR302	$\overline{\text{KBD IRQ}}$
CR303	$\overline{\text{KNOB IRQ}}$
CR304	$\overline{\text{FDB IRQ}}$
CR305	$\overline{\text{GPIB IRQ}}$

The sequence described above can be summarized briefly. An operator presses a keyboard switch, generating a low at pin 1 of inverter IC324. The inverted output goes through gate circuits (IC316 and IC314) to the microprocessor (the $\overline{\text{IRQ}}$ signal) and also goes to CK1 of IC311 where it appears at the $\overline{\text{Q1}}$ output (pin 6) and at pin 2 of IC322 as a low. The microprocessor provides outputs to set the NAND gates in IC320 to enable IC322 and read the status of the information on its input pins and determine which interrupt needs to be serviced. The microprocessor performs the necessary service routines and then enables latch IC310 to reset all appropriate circuitry to await the next interrupt.

8.5.6.5 The other 4 buffer/line drivers in IC322 (with inputs at pins 11, 13, 15, and 17) are enabled when the AutoCal® switch on the rear panel is in the AutoCal® position. Decode logic through IC320 enables this half of IC322 and sends AutoCal® (pin 9) and GPIB mode (pin 5) information to the microprocessor over data/address lines B0 - B3. Switch SW301 selects the ROM memory bank (IC306) associated with the AutoCal® routine.

8.5.6.6 Regulator IC325 provides the regulated +5 VDC used on the microprocessor board.

8.5.7 OSCILLATOR BOARD, MAIN LOCK AND VCO

The schematic for the Main Lock and VCO section of the Oscillator Board (Figure 10-8, sheet 1 of schematic number 0014-30-0355) contains the Main

Loop phase detector, the loop unlock/over modulation indicator circuitry, the APC (Automatic Phase Control) comparator circuitry, the frequency coarse tuning circuitry, FM circuitry, and oscillators 1-4 (the VCO group) and associated circuitry.

8.5.7.1 Phase detector IC502 compares the Main Reference 1 MHz to the 1 MHz Main Loop Fractional Frequency Divider Output (see Section 8.5.1 and 8.5.3, respectively, for more detail about the origin of these signals) and generates an error signal, as appropriate, at pin 1 of op amp IC503A. This error signal is summed at pin 5 of op amp IC503B with the coarse tuning output from Digital-to-Analog Converter (DAC) IC506 (at pin 6 of IC503B) to provide the varactor drive voltage for the VCO group (oscillators 1-4).

8.5.7.2 The error signal at pin 1 of IC503A also is applied to pins 9 and 10 of op amp IC504C. The output at pin 8 is the Main Loop Unlock line back to the microprocessor. Normally low, the line goes high (logic 1) when the main loop becomes unlocked. A low at either pin 2 or 3 of IC503A will generate a Main Loop Unlock signal (high) at pin 8 of IC504C.

8.5.7.3 The error signal at pin 1 of IC503A also is applied to pins 12 and 13 of op amp IC504D. The output at pin 14 of IC504D is fed to pin 3 of op amp IC504A where it is compared to the reference voltage at pin 2. The output at pin 1 of IC504A provides the over modulation (over deviation) signal to the microprocessor. This line is normally low, going high (logic 1) when over modulation occurs.

8.5.7.4 The error signal at pin 1 of IC503A also is applied to pin 6 of op amp IC504B where it provides a voltage level that is compared to the ground reference at pin 5. The output at pin 7 is the Automatic Phase Control (APC) comparator line that is read by the microprocessor only during the frequency calibration portion of the Auto Cal® procedure. During the frequency calibration routine, the microprocessor stores the binary control words associated with each calibration point. These points are identified as the voltage level at pin 6 of IC504B crosses (alternately goes above and then goes below) the zero volt reference at pin 5. (The coarse tuning word to DAC IC506 is stored in response to the APC comparator signal when the zero reference is crossed.)

8.5.7.5 The coarse tune DAC (IC506) is a 10-bit device that generates an output to pin 6 of IC503B in response to the frequency control word from the microprocessor (at J501). The DAC output is summed with the Main Loop error signal from Main Loop phase detector IC502 to provide the varactor drive for the oscillators on this board. The output from pin 7 of IC503B is the varactor drive.

When FM is not required, SW3 of Analog Switch IC507 is on and R526 (6.2 MΩ) is not in the circuit. The drive output from pin 7 of IC503B goes through R525, SW3 from S3 to D3 of IC507, and through R660 to the varactors in each oscillator circuit. When an FM signal is used, SW3 of IC507 is off and the drive signal must go through R526. When the much smaller resistance of R525 (12 kΩ) is replaced by the 6.2 MΩ of R526, the circuit becomes essentially an RC network (R526, R660, C521, and R528) with a relatively large R component and the main loop speed is slowed by the change in R value.

8.5.7.6 Analog Switch IC507 allows the FM signal to add to the varactor drive. The DG303 truth table shown on the schematic applies to this analog switch. When the "IN" signal to IC507 (the FM Enable from the Main Board) is low, no FM is present. SW1 and SW2 of IC507 are off and therefore their connections from S1 to D1 and from S2 to D2 are open. SW3 is on and operates

as described above. When the FM enable is high (logic 1), SW1 and SW2 are on. SW2 allows the FM signal at D2 (pin 10) to pass through to S2 (pin 11) and then add to the varactor drive. When S1 and D1 of SW1 are connected, the high pass network in front of IC503B (pin 5) is changed and prevents the loop from being underdamped by the gain reduction of R526.

8.5.7.7 The varactor drive from pin 7 of IC503B can range from 2 to 13 volts and is applied to varactor input circuitry for each of oscillators 1 - 4. The higher the voltage applied, the higher the output frequency from each oscillator. The actual voltage range required to provide the frequency range for each oscillator (shown in Section 8.5.7.7.2) will be less than from 2 to 13 volts. For example, oscillator number 1 may cover its frequency range with a voltage input from 2 to 7 volts. Oscillator number 4 may require a 5 to 12 volts input to cover its frequency range.

8.5.7.7.1 Quad Analog Switch IC501 provides the decode logic at outputs 1 - 4 to select which oscillator is enabled (output A = Osc 1; output B = Osc 2; etc.) according to the select inputs at J501. A -12 volt output enables an oscillator. The output is greater than -1 volt when an oscillator is turned off. For example, when oscillator 1 is enabled, output 1 at pin 2 will be at -12 volts and will be applied at the junction of C501 and R542, as shown ("A" to "A" connection). The other three outputs of IC501 will be set at greater than -1 volt. The inputs to IC501 are active low.

8.5.7.7.2 The range for each oscillator as shown on the schematic is:

Oscillator	Range
1	275 - 327 MHz
2	327 - 389 MHz
3	389 - 463 MHz
4	463 - 550 MHz

The ranges are determined by the varactor diode network, transmission line segment, and base capacitors associated with each oscillator (Q501 - Q504). The varactor diodes associated with oscillator 1 (Q501) are CR506 - CR509. The capacitive reactance in this network is changed to inductive reactance by the transmission line segment that immediately follows the varactors. The reactance forms an LC resonant circuit with capacitors C533 and C534. This circuit determines the frequency range for oscillator 1. The frequency ranges for oscillators 2 - 4 are determined by their corresponding circuit components.

8.5.7.7.3 The capacitor network following each oscillator (C535 to C537 for oscillator 1) is a low pass filter network to get rid of harmonics. The output from the particular oscillator that has been enabled is fed to RF output amplifiers shown on Figure 10-9.

8.5.8 OSCILLATOR BOARD, LEVELER AND LOCAL OSCILLATOR LOCK

The schematic for the Leveler and Local Oscillator (L.O.) Lock section of the Oscillator Board (Figure 10-9, sheet 2 of schematic number 0014-30-0355) contains amplifiers and a leveler for the RF output from the VCO group (see 8.5.7.7.3, above) and also contains phase detector circuitry and the unlock indicator circuitry for the Local Oscillator Loop.

8.5.8.1 The RF signal from the VCO group (oscillator 1, for example) comes in at line 1E on Figure 10-9 and goes through amplifiers and a leveler circuit before it is sent to the RF Amplifier Board (J505) and to the Main Loop Divider (J504).

8.5.8.1.1 Transistor Q505 amplifies the RF signal to the Amplifier Board. Transistor Q513 provides a stable bias for Q505. RF detector CR533 generates a DC voltage level proportional to the RF amplifier output. This DC level is

applied to the DC amplifier IC514B in the leveler circuit. The voltage output at pin 7 of IC514B controls the current through diode attenuator CR531 to maintain a fixed RF level out to the Amplifier Board at J505 (a nominal drive output of 2 dBm).

8.5.8.1.2 The RF signal out to the Main Loop Divider (at J504) goes through the two stages of amplification shown on Figure 10-9. Transistor Q506 and then transistor pair Q514 and Q507 provide amplification to produce an output at J504 of a nominal +10 dBm.

8.5.8.2 Local Oscillator (L.O.) Loop Phase Detector IC509 receives the 1 MHz reference at pin 1 and the 1 MHz L.O. divider signal at pin 3.

8.5.8.2.1 The resultant error signal at pin 1 of op amp IC508A provides the "TUNING" signal sent to the Local Oscillator Board (Figure 10-10) and sent to op amp IC508B. IC508A is used as a loop filter. IC508B is used as a window detector. If the Tuning Signal from IC508A is less than 0 volt or greater than ~ 10 volts, it generates the L.O. unlock indicator at pin 25 of J501. The unlock line is low when the local oscillator loop is locked. It goes high when the loop becomes unlocked.

8.5.8.2.2 The L.O. enable from the Main Board (see Section 8.5.4) turns on transistor Q515 and allows the unlock detector to function. The L.O. enable also is applied to the Local Oscillator Board (Figure 10-10) as the "LO EN" signal.

8.5.8.3 Regulators IC512, IC510, and IC511 provide on-card regulation for the +15 VDC, -15 VDC, and +5 VDC power used on the Oscillator Board.

8.5.9 LOCAL OSCILLATOR BOARD

Local Oscillator Board components are shown in Figure 10-10.

8.5.9.1 Transistors Q511 and Q512 are controlled by the L.O. enable signal and provide bias for oscillator Q508.

8.5.9.2 The "TUNING" signal (the error voltage from the Local Oscillator phase detector on Figure 10-9) is applied to CR522 across the filter network shown. The output at the collector of Q508 passes through a low pass filter and is applied to the bases of amplifiers Q509 and Q510.

8.5.9.2.1 The output at the collector of Q509 is the Local Oscillator 500 MHz to the Amplifier Board of the RF Module (see Figure 8-1).

8.5.9.2.2 The output at the collector of Q510 is the Local Oscillator 500 MHz to the divide-by-500 (÷ 500) Local Oscillator Divider Network (see Figure 8-1).

8.5.9.3 The RLC networks following the outputs of Q509 and Q510 are bias decoupling networks.

8.5.10 AMPLIFIER ASSEMBLY, FREQUENCY CONVERSION SECTION

Figure 8-8 shows the RF Amplifier Assembly and its inputs and outputs (I/O). The frequency conversion section of the Amplifier Assembly is shown on Figure 10-11, sheet 1 of the Amplifier Board schematic (0014-30-0363). This schematic shows the four paths the RF IN signal can take, depending upon the desired output frequency, and also shows the microprocessor band switch control network that determines the path the signal will take.

8.5.10.1 The four pathways the 275 - 550 MHz RF In signal can take through the frequency conversion circuitry are shown in simplified form in Figure 8-9. Path 1 is the frequency doubler circuit and contains three branches (H1 - H3). Path 2 is the divide-by-two circuit and contains two branches (L2 and L3). The branches in the two multibranch

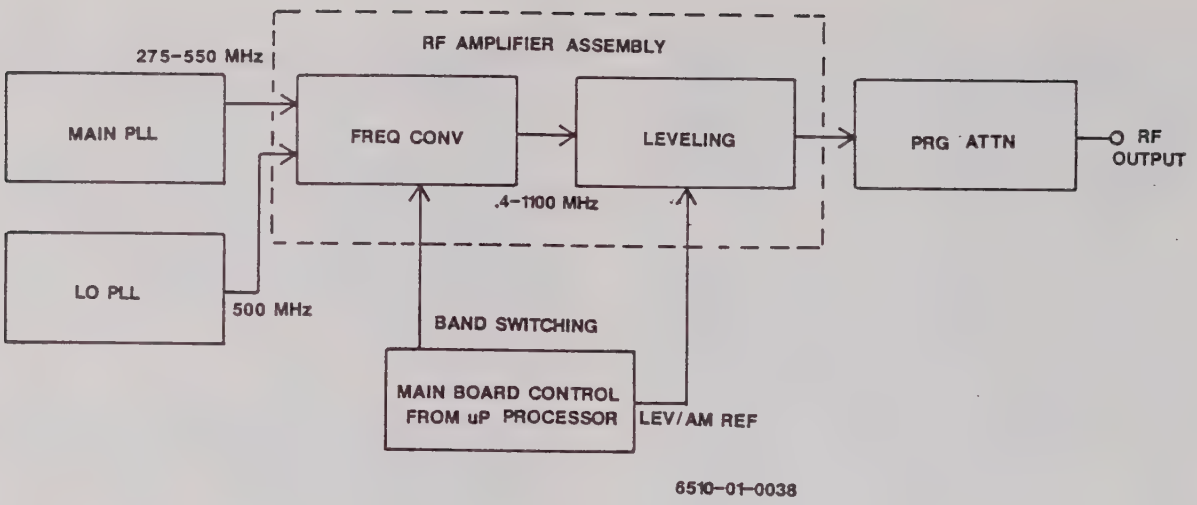


Figure 8-8. Block Diagram, RF Amplifier Assembly and I/O

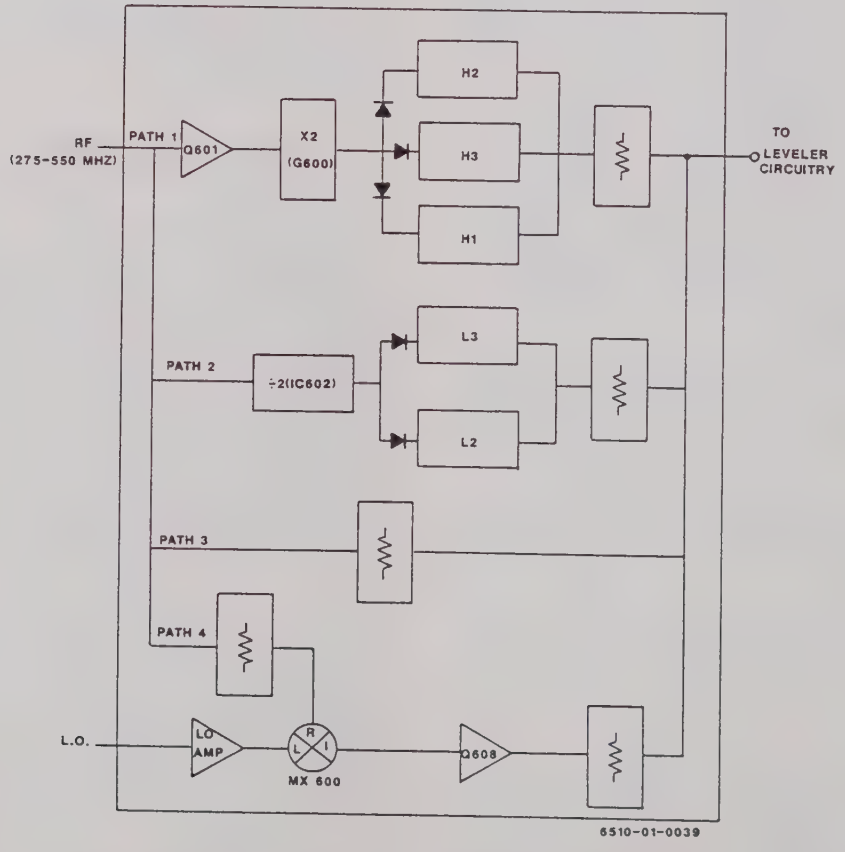


Figure 8-9. Block Diagram, RF Amplifier Assembly Frequency Conversion Pathways

circuits are identified on Figure 8-9 by the band switching signals that open them for signal flow. Path 3 is the straight through, no conversion circuit. Path 4 is the pathway where the RF signal is heterodyned with the 500 MHz from the local oscillator. Each path is described in greater detail in the following paragraphs.

8.5.10.2 Refer to Figure 10-11. Signal path 1 begins through diode CR601 to amplifier transistor Q601 of the frequency doubler circuit. Path 2 begins through CR600 and CR612 to the divide-by-two prescaler IC602. Path 3 is the sole non-conversion route and begins through diodes CR600, CR611, and CR625. Path 4 begins through diodes CR600 and CR610 into mixer MX600.

8.5.10.3 The RF signal in from the Oscillator Assembly at J601 will be applied simultaneously to each path described above. Only one path will be opened (turned on). The actual path the signal takes will be determined by the band switching control signals from the microprocessor (via the main board) at J603. The band switching signals control circuitry (transistors Q610, Q612 and hex bus driver IC601) to turn on diodes and other components in each path to allow signal flow. Band switching signals are positive logic (1 = 5 volts), with all lines active high. The truth table and frequencies associated with the band switching control signals are shown in Table 8-4.

8.5.10.4 The diodes controlled (turned on/off) by each band switching signal are shown in Table 8-5.

Band switching signal L5 turns on transistor Q605 to supply base current to Q604. When Q604 conducts, the 8 volt supply at pin 19 of J603 will be applied to pin 3 of 5 volt regulator IC603. The regulated 5 volt output at pin 1 supplies the divide-by-two network.

Band switching signal GCEN turns on Q603 to provide base current for Q602 and feed the +12 volt from the Leveler Section of the Amp Board to the frequency doubler network.

8.5.10.5 Transistor amplifier Q601 in the frequency doubler network is controlled by Q600 and band switching signal GCEN. The amplified RF in signal from J601 is applied to frequency doubler G600 and then goes to the three topmost tuned LC strings shown on Figure 10-11. The top string shown on the figure (from CR604 to L605, C619, L611, etc.) is controlled by band switching signal H2 and provides an output to the Leveler Section from 695 MHz to 875 MHz. Coils L608, L611, and L614 are adjusted at the factory for optimum output response in this range. The second string shown (from CR605 to L609, C620, L612, etc.) is controlled by band switching signal H3 and provides an output from 875 MHz to 1100 MHz. Coils L609, L612, and L615 are adjusted for optimum output response. The third string shown (from CR603 to L610, C621, L613, etc.) is controlled by signal H1 and provides an output from 550 MHz to 695 MHz. Coils L610, L613, and L617 are adjusted for optimum output response. The output from the string turned on (by H2, H3, or H1 and GCEN) is the "LEVELER RF IN" signal to the Leveler Section.

8.5.10.6 Prescaler IC602 is the divide-by-two device that supplies a counted down version of the RF IN signal at J601 to the two LC low pass filter strings in the divide-by-two network. The string from CR613 to L628, L630, and L632 is controlled by band switching signal L3 and provides an output from 195 MHz to 275 MHz. The string from CR614 to L629, L631, and L633 is controlled by signal L2 and provides an output from 137.5 MHz to 195 MHz. The output from the string turned on (by L3 or L2 and L5) is fed through CR617 and is the "LEVELER RF IN" signal to the Leveler Section.

TABLE 8-4.
BAND SWITCHING SIGNAL TRUTH TABLE

OUTPUT FREQUENCY (MHz)	BAND SWITCHING CONTROL SIGNAL								
	L1	L2	L3	L4	L5	GCEN	H1	H2	H3
4-137.5	1	0	0	0	0	0	0	0	0
137.5-195	0	1	0	0	1	0	0	0	0
195-275	0	0	1	0	1	0	0	0	0
275-550	0	0	0	1	0	0	0	0	0
550-693	0	0	0	0	0	1	1	0	0
693-873	0	0	0	0	0	1	0	1	0
873-1100	0	0	0	0	0	1	0	0	1

TABLE 8-5.
BAND SWITCHING SIGNAL/DIODE RELATIONSHIP

Diode	BAND SWITCHING CONTROL SIGNAL						
	L1	L2	L3	L4	H1	H2	H3
CR600	x	x	x	x			
CR601					x	x	x
CR603					x		
CR604						x	
CR605							x
CR606							x
CR607					x		
CR608					x	x	x
CR609	x	x	x	x			
CR610	x						
CR611				x			
CR612		x	x				
CR613			x				
CR614		x					
CR615			x				
CR616		x					
CR617		x	x				
CR618	x			x			
CR619	x						
CR621						x	
CR622				x			
CR623	x						
CR625				x			

8.5.10.7 The path through CR600, CR611, and the circuitry following these diodes is essentially the straight through, non-conversion path for the RF IN at J601. Band switching signal L4 turns on amplifier Q610 to provide a base current for Q609 and turn on the diodes that control signal flow through this path. The 275 MHz to 550 MHz output is the "LEVELER RF IN" to the Leveler Section.

8.5.10.8 The final path the RF IN signal at J601 may take is through CR610 into mixer MX600. The "Local Oscillator In" (a 500 MHz signal) at J602 is amplified by transistor Q606 and then applied to the mixer. The mixer output goes to the low pass filter (L647, L648, and associated capacitors) through Q608. Q608 is controlled by the L2 band switching signal as it turns on Q612 and Q611. The output of 0.4 MHz - 137.5 MHz across the low pass filter is applied to CR623 and eventually to the Leveler Section as shown. Transistor Q607 provides bias for Q606.

8.5.11 AMPLIFIER ASSEMBLY, LEVELER SECTION

The leveler section of the RF Amplifier Module is shown in schematic form on Figure 10-12, sheet 2 of the Amp Board schematic (0013-30-0363) and in simplified form on Figure 8-10. Coarse level control is performed by PIN diode attenuators CR701 and CR702. Fine level control is accomplished by PIN diode attenuators CR703 and CR704.

8.5.11.1 The coarse level control PIN diode attenuators (CR701 and CR702; see Figure 10-12) are driven through transistors Q709 and Q707 by the AM/LEV drive reference (pin 3 of J603) from the carrier level and modulation control circuitry on the main board (see Figure 8-1 and Section 8.5.2.3). Transistors Q709 and Q707 form a voltage level shifting device that controls the current through the PIN diodes to set the coarse RF signal level before it goes to the fine control portion of the leveling loop.

8.5.11.2 A feedback system is used to achieve fine level control. The RF output to J600 is detected by diode CR707 and the detected signal fed to summing amplifier IC701A (pin 2). IC701A and op amp IC701B and their associated circuitry provide linearity correction for detector CR707. Diode CR709 supplies a temperature compensation input to this circuit. Potentiometers R757 and R767 are the zero adjust and +3 dBm adjust pots, respectively. The linearized output is applied to pin 6 of comparator IC700B where it is compared to the AM/LEV drive reference (pin 3 of J603) from the carrier level and modulation control circuitry on the Main Board (see Figure 8-1 and Section 8.5.2.3). The resultant error signal at pin 7 of IC700B is applied to the base of Q708, producing a voltage change that controls the current through PIN diodes CR703 and CR704.

8.5.11.2.1 The error signal also is fed to pins 2 and 3 of IC700A to generate an unlevel indication at pin 1 if the input error signal is less than 0 volt or greater than +12 volts.

8.5.11.2.2 The AM/LEV return line at pin 4 of J603 provides a common ground for the AM/LEV drive reference on the amp board and the main board.

8.5.11.2.3 The RF MON line at pin 7 of J603 provides an RF out test point for the amp board.

8.5.11.3 Amplitude modulation is achieved by superimposing a modulation signal on top of the DC level reference voltage in the AM/LEV drive signal. The amplitude of the RF out signal will track the AM input.

8.5.11.4 Transistors Q700, Q701, Q702, Q704 and Q706 amplify the RF signal.

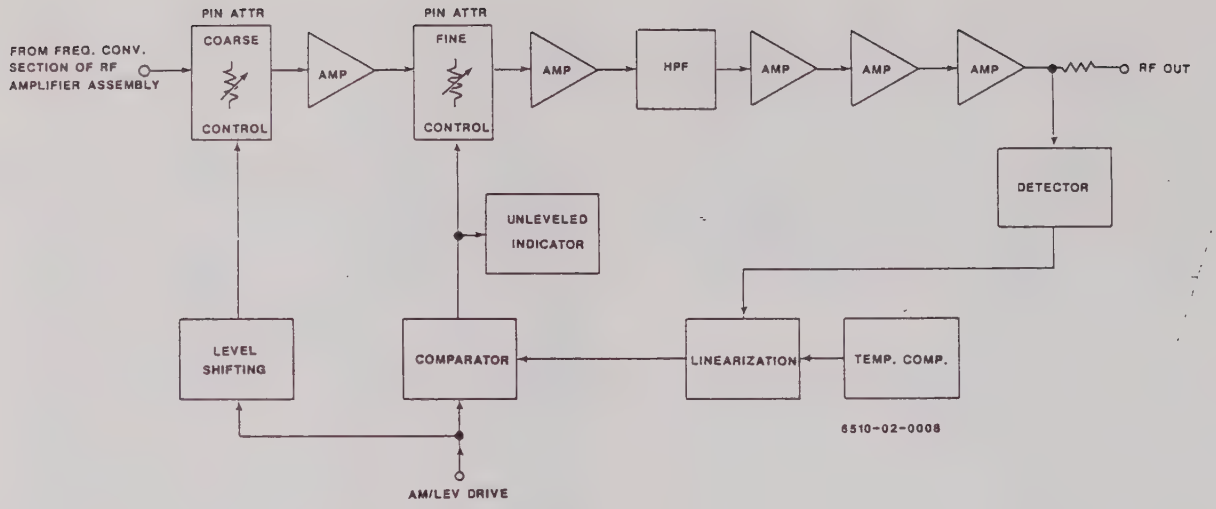


Figure 8-10. Block Diagram, RF Amplifier Assembly Leveler Circuitry

Coils L704, L709, L710, L712, and L723 are tuned for optimum frequency response over the range of the instrument (0.4 MHz to 1100 MHz). The high pass filter (HPF; C708, C710, and L707) removes any signal component less than 200 kHz.

8.5.11.5 The output RF level at J600 is calibrated in terms of the AM/LEV drive such that

$$V_{AM/LEV} = 8 \times V_0$$

where the AM/LEV voltage is DC and the output voltage (V_0) is the RMS value across a 50Ω load (measured at the Amplifier Assembly output connector).

An 8 VDC AM/LEV drive input, for example, will produce a 1 VRMS output signal:

$$8 = 8 \times V_0$$
$$V_0 = 1 \text{ Volt RMS}$$

This 1 Volt RMS output signal is equivalent to a power level of +13 dBm.

8.5.11.6 The relationship between AM depth and the AM/LEV reference voltage input is:

$$m = 100\% \times \frac{1.414 \times VAC}{VDC}$$

where m is the modulation depth, VAC is the AC component of the AM/LEV drive (RMS value) and VDC is the DC component of the AM/LEV drive.

The relationships between output power level (P_0) in dBm and the DC and AC reference voltages at 30%, 70%, and 90% AM for several commonly used power settings are shown in Table 8-6.

8.5.11.7 IC702, IC703, and IC704 provide the regulated +12 VDC, +15 VDC, and -15 VDC power, respectively, used on the Amp Board.

8.5.12 DISPLAY BOARD, LCD AND DECODE LOGIC CIRCUITRY

The circuitry associated with the front panel LCDs (Liquid Crystal Displays) is shown on Figure 10-13, sheet 1 of 2 for the Display Board schematic (0014-30-0351). This schematic also shows decode logic for microprocessor/front panel communication.

8.5.12.1 Decoder (1 of 8) IC808 provides enables at outputs Y7-Y0 (pins 7,

TABLE 8-6.
MODULATION DEPTH/POWER OUT/VOLTAGE RELATIONSHIPS

P_O dBm	VDC V	VAC (VRMS) m = 30%	m = 70%	m = 90%
+13	7.99	1.695	3.955	5.086
+9	5.04	1.069	2.497	3.210
+6	3.57	0.757	1.767	2.272
+3	2.53	0.537	1.252	1.610
0	1.79	0.380	0.885	1.139
-4	1.13	0.239	0.559	0.718
-7	0.799	0.170	0.396	0.508
-10	0.566	0.120	0.280	0.360
-13	0.400	0.085	0.198	0.255

9 - 15) for the LCD interface/drivers IC801 - IC807, shift register IC810, 2-D type flip-flop IC814, and microprocessor communication gates in IC811 and IC812. Clock and $\overline{CKEN}$ signals from the microprocessor (J801) provide the chip selects to IC808 (pins 5 and 6). Clock selects 0 - 2 are decoded by IC808.

8.5.12.2 IC810 is an 8-bit serial input/parallel output shift register that receives serial data at pin 1 (A IN) and provides chip selects for the LCD drivers at outputs 0A - 0G (pins 3 - 6 and 10 - 12). IC810 is enabled at pin 8.

8.5.12.3 The LCD interface/driver chips (IC801 - IC807) are 40-bit shift registers that turn on their associated LCD elements according to the patterns shown for each driver (IC1 - IC7) in the table on Figure 10-13. The 40 bits of data to each driver are translated inside the driver to produce the required display.

8.5.12.4 The three LCDs (DPS801 - DPS803) are triplex custom displays with three back planes. To turn on an element in a display also requires its associated back plane (one of the three) to be turned on. Back plane coding also is performed inside the LCD interface/drivers. Note that three interface drivers are associated with the FREQUENCY LCD as opposed to only two drivers for the LEVEL and MODULATION LCDs.

8.5.12.5 The backlights (BL801- BL803) for the three LCDs are enabled by the Q output at pin 9 of flip-flop IC814. The low generated here is sent to the power supply to enable the 125 VAC input from the Power Supply to each backlight package (see Section 8.5.5.9 of this manual for greater detail).

8.5.13 DISPLAY BOARD, SPIN KNOB

Sheet 2 of 2 for the Display Board schematic (Figure 10-14) includes the circuitry to process data from the front panel spin knob and the keyboard switches. The discussion of the circuitry associated with the keyboard is included with the description of the keyboard matrix in the next section (8.5.14).

8.5.13.1 The front panel spin knob essentially contains a two switch rotary encoder that sends the two signals shown in Figure 8-11 to J804

(pins 1 and 2) that produce the spin knob interrupt request (KNOB IRQ) and also tell the microprocessor whether the spin knob is being turned in the direction to increase or decrease (UP/DOWN) the value of the characteristic it controls.

8.5.13.2 The clock pulses from the spin knob (pin 1 of J804) are fed through NAND Schmitt Trigger IC812 from pins 12 and 13 to pin 11 at the same time direction information (high/low) is fed through pins 9 and 10 to pin 8 of IC812. The clock and direction pulse trains shown in Figure 8-11 are hardware generated as the spin knob is turned. The two trains are 90° out of phase. Turning the knob in a clockwise (CW) direction will product a different set of rising edges on the clock pulses and a different associated voltage level for the direction pulses than will be produced by counterclockwise (CCW) rotation of the knob. With clockwise rotation the rising clock edges at u1, u2, u3, and u4 will be associated with a 5 volt direction level. With counter clockwise rotation the rising clock edges become d1, d2, d3, and d4 and are associated with the 0 volt direction level. The clock pulses from pin 11 are applied to pin 3 of D-type flip-flop IC814. The direction information from pin 8 of IC812 is applied to pin 2 of IC814 and clocked through to pin 6 of IC814 with each rising clock edge at pin 3. A high at pin 6 tells the microprocessor that the spin knob is being turned to increase (UP) the value of the controlled characteristic. A low at pin 6 indicates the characteristic is to decrease (DOWN).

8.5.13.3 The direction signal from pin 8 of IC812 is applied to pin 2 of dual flip-flop IC813. The inverted output at pin 5 is applied to pin 12 of IC813 and then clocked through to pin 8 by knob clock pulses at pin 3 and 11 of IC813. The dual outputs (from pins 5 and 8) are fed to NAND Schmitt Trigger IC812 at pins 5 and 4, respectively, to generate the KNOB IRQ signal at pin 6.

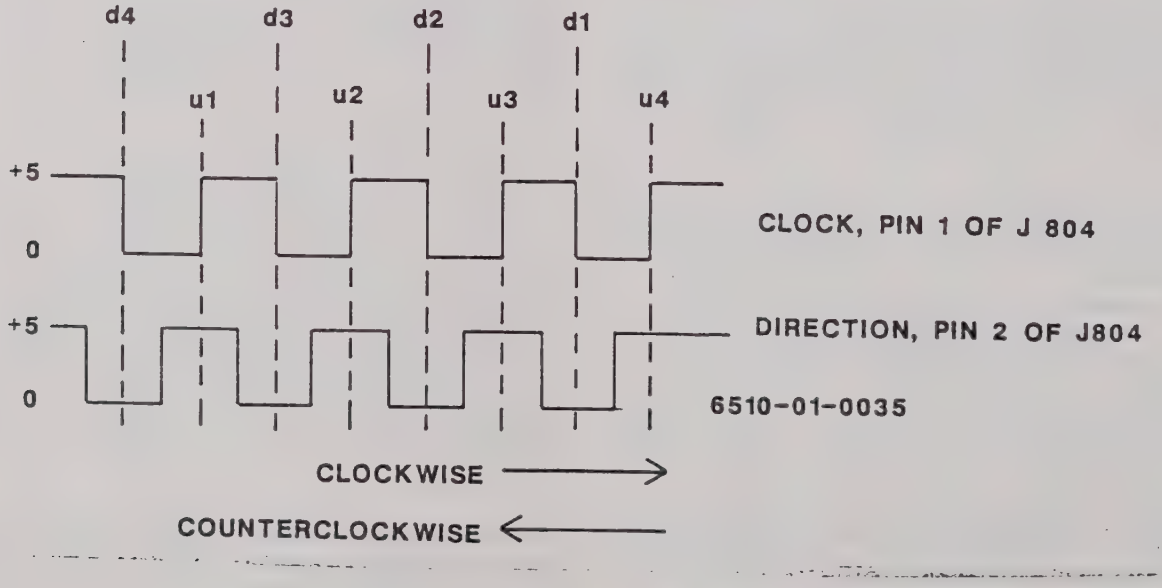


Figure 8-11. Spin Knob Clock/Direction Signals.

8.5.13.4 The pulse trains (pins 1 and 2 of J804) from the spin knob are mechanically generated using wipers inside the rotary encoder. Resistor R803 provides a path to ground for pins 12 and 13 of IC812 when the clock pulse encoder switch is open. Capacitor C819 helps debounce the switch, debouncing signal voltage changes. Resistor R802 and capacitor C818 perform the same function for the direction information pulse train at pin 2 of J804. The Schmitt triggers of IC812 provide additional debouncing for signal voltage level changes.

8.5.14 KEYBOARD CIRCUITRY

When a keyboard switch is pressed, the keyboard interrupt request ($\overline{\text{KBD IRQ}}$) is generated and the microprocessor initiates the data exchange necessary to identify the particular key that generated the request for service. The decode process description involves two schematics, the Keyboard schematic (Figure 10-15) and sheet 2 of the Display Board schematic, Figure 10-14.

8.5.14.1 During operation between keyboard use, the microprocessor sets a logic "0" (low; o volts) at pins 1 - 8 of P803. The voltage at pins 9 - 13 of P803 is a logic "1" (high; +5 volts) because these pins are connect to +5 volts through the pull-up resister network RN801 shown on Figure 10-14.

8.5.14.2 Pressing any keyboard switch connects the associated column (pins 9 - 13 of P803; see Figure 10-15) to the low at the row (pins 1 - 8 of P803) to which the column is connected when the switch is pressed. The low at the column is fed through J803 (Figure 10-14) to the associated pin input to AND gate IC818 where it generates a low output at pin 12 of IC818. This signal is the $\overline{\text{KBD IRQ}}$ that tells the microprocessor the keyboard requires service.

8.5.14.3 The microprocessor will send a stream of serial data out to 8-bit serial input/parallel output shift register IC816 to identify the row in which the pressed keyboard switch is located. The "keyboard in" clock at pin 8 of IC816 will clock the data through. Switch matrix decoding is shown on Figure 10-15. The microprocessor sets all rows except one equal to a logic "1". The row that is not set at a "1" is set at a "0". One row at a time, from row 0 to row 7, is sequentially set equal to logic "0" in a series of 8-bit bytes. If it is row 0 that is set at logic "0" and the pressed switch is in row 0 (S1, for example), the low (logic "0") at row 0 will pass through S1 to column 2 pin 9 (P803 and J803) to pin 13 of shift register IC817 (an 8-bit parallel input/serial output device). The remaining column inputs to IC817 (pins 14, 3, 4, and 5) will be high. The status of the column input lines will be clocked out of IC817 (pin 9) by the keyboard out clock at pin 2 in a serial stream back to the microprocessor to identify the row.

8.5.14.4 If the pressed switch had been in row 2 (S12, for example), setting row 0 or row 1 (or rows 3 - 7) at a logic "0" will not allow a low to be input to IC817. All "1"s will be input because column 3 in which S12 is located will be set at "1" by the microprocessor while columns 2 and 4 - 6 will be high because of the +5 volt pull-up resistors (RN801). The microprocessor will sequentially clock the "0" and seven "1"s in 8-bit bytes (as shown on Figure 10-15) onto the rows until the row in which the pressed switch is located is identified.

8.5.14.5 The column in which the switch is located will be found by setting all row outputs from IC816 equal to a logic "0" and reading the single column at which the low appears into IC817 (either pin 13, 14, 3, 4, or 5). Column information also is provided as an 8-bit byte of data. The pull-up resistor network will maintain highs (logic 1) at all column inputs except

the one with the closed (pressed) switch (which will be connected to the one of the lows out of IC816).

8.5.14.6 The 8-bit bytes used to identify the row and column in which each switch is located are shown in a table on Figure 10-15.

8.5.15 PROGRAMMABLE ATTENUATOR

The programmable attenuator (see Figure 8-12) contains six attenuator pads, a reverse power detector, and a reverse power relay (breaker). The RF in signal from J600 of the RF Amplifier Module goes through the pad network selected by control signals from the microprocessor via main board P103 (see Section 8.5.2.4) into and through the attenuator relay.

8.5.15.1 The relay is held on by a +12 volt signal (S1) from the reverse power protection circuit on the main board (see Section 8.5.2.5). RF out of the relay is fed to the RF out connector on the 2500 front panel.

8.5.15.2 If an RF power source is inadvertently attached to the RF output, the reverse power detector detects the input and sends a signal to the reverse power protection circuit to trigger the circuit as described in Section 8.5.2.5.

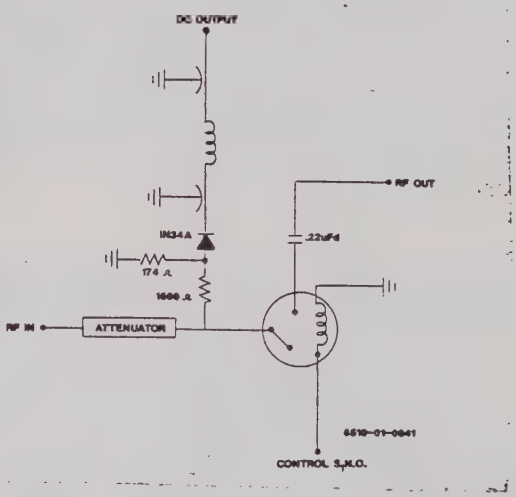


Figure 8-12. Schematic, Programmable Attenuator

9.1 INTRODUCTION

No troubleshooting guide can replace the knowledge and skills of experienced repair personnel. The purpose of this guide is to provide information to help the troubleshooter isolate the cause of an instrument failure, correct the problem, and return the unit to normal service as soon as possible. This guide also provides a general methodology for troubleshooting. Some failures are easily corrected while others may require a thorough understanding of the block diagrams and circuit descriptions in Section 8 of this Service Manual. Successful troubleshooting is based on understanding circuit operation within and between unit subassemblies. Therefore the troubleshooter should be familiar with functional and detailed circuit descriptions and the schematics for this unit.

When the instrument is operating, but out of specifications (Section 1.2 of the Operating Manual), performing the AutoCal® calibration procedure in Section 5.3 of the Operating Manual may correct the problem.

9.1.1 INITIAL PREPARATION

Before attempting to troubleshoot the Model 2500, please read the Theory of Operation in Section 8 of this manual. Signal flow through the unit is traced in detail, with subassembly inputs and outputs clearly identified. The troubleshooter should be familiar with the relevant performance test procedures and maintenance procedures (especially the user diagnostics) detailed in Sections 4 and 5, respectively, of the Operating Manual.

9.1.2 METHODOLOGY

Troubleshooting is, in general, a systematic process of elimination. A thorough understanding of the circuit descriptions located in Section 8 of this manual will enable the trouble symptom to be associated with a particular circuit function. Once this has been accomplished, the problem can be further isolated using the reference schematics in Section 10. Voltage and resistance checks may then be used to locate the defective component.

9.1.3 FACTORY REPAIR

Wavetek maintains an on-site staff of highly skilled, experienced electronic technicians to provide assistance for those customers who lack the necessary test equipment or personnel to troubleshoot/repair the unit. Please obtain factory authorization before returning a unit for repair. If a unit is returned for repair, please include a detailed description of the problem encountered (to minimize turnaround time).

9.1.4 RECOMMENDED TEST EQUIPMENT

Recommended troubleshooting test equipment is listed in Table 9-1.

TABLE 9-1.
RECOMMENDED TEST EQUIPMENT

INSTRUMENT	RECOMMENDED
Signal Generator	Wavetek Model 2500 or equivalent
Oscilloscope	Tektronix 465 or equivalent, with matched X10 probes
Frequency Counter	Hewlett-Packard Model 5383A with external reference time base accuracy of ±5 parts in 10^8, or equivalent
Digital Voltmeter	Fluke Model 8010A, or equivalent
Spectrum Analyzer	Tektronix 496, 492, or equivalent Hewlett-Packard 8559A, or equivalent
Spectrum Analyzer	Hewlett-Packard 8568, or equivalent
Modulation Analyzer	H-P 8901A (if an equivalent is used a counter may be needed)
Measurement Receiver	H-P 8902A, with sensor module 11722A, or equivalent
Power Meter	H-P 436A, with Power Sensor 8482A, or equivalent
Function Generator	Wavetek Model 20 or equivalent
Audio Analyzer	H-P 8903A, or equivalent
VSWR Bridge	Wiltron Model 60N50, or equivalent
Sweep Generator	Wavetek Model 2002A, or equivalent

9.2 PERSONNEL SAFETY CONSIDERATIONS

Maintain the standard safety precautions required when working around 100-240 VAC. Be aware that when the top cover of the unit is removed, there is 120 VAC at the back of the display board.

9.3 INSTRUMENT SAFETY CONSIDERATIONS

Static sensitive devices are used in this instrument. Use ESD precautions when handling a static sensitive device or a card on which a static sensitive device is mounted. These devices may not fail catastrophically if precautions are not taken, but the life of the device and its performance may be reduced and an early failure may result.

9.4 INITIAL INSPECTION

Instrument problems sometimes have simple, fairly obvious, solutions that are apparent upon visual inspections. Perform the following inspections before proceeding with extensive troubleshooting.

9.4.1 INPUT POWER

Verify the unit is plugged into an appropriate power source and that the unit is turned on. Verify the voltage

selector (Section 2.4 of the Operating Manual) is set properly. Verify the fuse in the AC Power Connector Module (Section 2.4 of the Operating Manual) has not opened.

9.4.2 INCORRECT CONTROL SETTINGS

Verify a correct operating procedure has been used. Refer to Section 3 of the Operating Manual for a complete description of each front and rear panel control, display, and connector. Section 3 contains operating instructions for the unit.

9.4.3 VISUAL AND MECHANICAL CHECKS

Failures, whether they are continuous or intermittent, may be caused by any item listed in Table 9-2. The entire list may be checked out prior to further troubleshooting.

Note that units are shipped from the factory in operating condition. Some items on this checklist can occur because of improper handling during shipment and unpacking. Be aware that poor troubleshooting procedures can generate almost any of the items on the list.

TABLE 9-2.
VISUAL/MECHANICAL CHECKLIST

1. Loose RF Cables.
2. Loose cards (re-tightening securing screws may be helpful).
3. Improperly mated connectors.
4. Burned or broken components.
5. Loose or missing screws.
6. RF cables to incorrect connectors.
7. Defective ribbon cables.
8. Solder joints on connectors or PC cards defective.
9. Incorrect power selection and fuse (see 9.4.1).
10. Defective contacts on cable connectors.
11. Defective wiring harness.
12. Broken wires.

9.5 GENERAL TROUBLESHOOTING NOTES

9.5.1 POWER UP TESTS/DIAGNOSTICS

The power up tests and the user diagnostics described in Section 5 of the Operating Manual should be used as troubleshooting aids when possible.

9.5.2 TEST HOOK-UPS

RF cables can be disconnected from the oscillator and amplifier assembly connectors, and a power meter or spectrum analyzer connected directly to the connector for power level or frequency measurements.

9.6 REPAIR WORK CAUTIONS

9.6.1 CUSTOM COMPONENT REPLACEMENT

Reference schematic components that have a star (*) beside them are custom components. The value for the component, if shown, is its typical value and may or may not be its actual value. The actual values for custom components are determined at the factory during factory calibration. They are the values required to bring an individual unit into specification. Major repair of a subassembly may require a trial and error substitution for the custom components in related circuitry to recalibrate the unit.

9.6.2 ROUTINE REPAIR WORK CAUTIONS

Observe the standard precautions associated with any electronic instrumentation repair. For example:

- Make certain there are no solder shorts on any board.
- Check the pin 1 location of any IC that is removed and reinserted or replaced; make certain that the IC is inserted correctly.
- Make certain electrolytic capacitors are installed properly.

9.7 POWER SUPPLY, DPS2F

9.7.1 If the unit is totally inoperable, check the power supply. If the power supply voltages are acceptable, verify the microprocessor board and the system clocks are functional (Sections 9.9 and 9.10).

9.7.2 A power supply problem also may cause many seemingly unrelated symptoms. The power supply should be checked when a symptom(s) does not clearly indicate a specific trouble area.

9.8 ON-BOARD REGULATORS

A voltage level problem on the individual boards in this unit may be the result of a defective regulator or a defective electrolytic capacitor. Voltmeter tests with the power supply turned on will normally reveal any such problem.

9.9 MICROPROCESSOR BOARD

Microprocessor board circuitry controls much of the unit's operation. Proper operation of the board is indicated by the front panel displays during the automatic power up test (described in Section 5.5 of the Operating Manual). Erratic or nonsense operation may result if microprocessor circuitry is bad, or the unit may be totally inoperable.

9.9.1 Basic system timing is derived from the 4 MHz crystal on the microprocessor board. The microprocessor (IC301; Figure 10-7) provides the 1 MHz system clock and the clock enables used on the Main Board to generate the various clocks that provide timing for control functions. Control functions that are closely related share the same clock. A problem with a particular clock or clock enable will be reflected in the system(s) it processes. The 5 system clocks and their functions are shown in Section 9.10, following this section.

9.9.2 There are several control signals (R/$\overline{W}$, $\overline{IRQ}$, FP/$\overline{MAIN}$, SERIAL/$\overline{GPIB}$, etc) and address and bus lines that are required for proper system operation. Usually it is only necessary to verify these signals and lines are switching.

9.9.3 Memory is apportioned as shown in Section 8.5.6.3.3, earlier. A problem with the RF control circuitry, for example, may be solved by replacing IC308, the bottom bank of which has RF control memory.

9.9.4 The microprocessor board is very complicated. Carefully read Sections 8.5.6 through 8.5.6.6 before troubleshooting this board.

9.10 MAIN BOARD

The main board generates 5 data clocks (0-4), a strobe, and the data stream. Various control signals are generated on and routed through the board.

9.10.1 The clocks (0-4) are shown with their associated control functions in Table 9-3. The abbreviated name for a function is shown in parenthesis.

TABLE 9-3.
DATA CLOCKS

Clock 0 - Coarse Frequency Tuning
- VCO bandswitching (B1-B4)
- Frequency Converter bandswitching (L1-L4)
- 1 GHz bandswitching (H1-H3)
- 1 GHz enable (GC EN)

Clock 1 - Main Loop Divider Program (C_{DIV})

Clock 2 - FM enable (FM EN)
- External Modulation (C_{EXT})
- Internal Modulation (C_{INT})
- 1 kHz enable
- 400 Hz enable

Clock 3 - DDS programming

Clock 4 - Carrier Level Control
- Deviation Correction

9.10.2 Test each clock by depressing the front panel mode pushbutton shown in Table 9-4 and rapidly rotating the spin knob while observing the indicated test point on an oscilloscope:

TABLE 9-4.
DATA CLOCK TEST POINTS

Clock	Mode	Test Point
0	FREQ	IC113, pin 15
1	FREQ	IC113, pin 14
2	FREQ	IC113, pin 13
3	INT FM	IC113, pin 12
4	LVL	IC113, pin 11

9.10.2.1 The data stream (IC114, pin 15) may be checked in any mode while rotating the spin knob.

9.10.2.2 The strobe (IC113, pin 7 or P104, p 8) may be checked in any mode while rotating the spin knob.

9.10.3 The $\overline{\text{FDB IRG}}$ signal is an error signal sent to the microprocessor. The $\overline{\text{FDB IRQ}}$ function may be tested by grounding all analog error indicator lines (simulating the normal, inactive state), then setting each line separately to +5 V. This simulates a detected error, and should send the FDB IRQ signal to the microprocessor section.

To perform the test, lift J101 pin 14 (Main Loop Unlock) from ground and apply 5 V. All other interrupt inputs must remain grounded. Observe transition to Logic zero at IC115 pin 13. Perform the same test for each of the error indicator lines: L.O. UNLOCK, APC COMP, OVER DEV., UNLEVEL.

9.10.4 Modulation sources and reference frequencies may be verified as follows:

9.10.4.1 With the rear panel select switch at "INT", observe a 10 MHz square wave at IC101, pin 1.

9.10.4.2 With a 10 MHz, 1 Vpp sinewave external reference input and the rear panel switch set at "EXT 10", observe a 10 MHz, 5 V square wave at IC110, pin 3. Observe a 1 MHz square wave reference at IC110, pin 8.

9.10.4.3 Repeat step 9.10.4.2 with external references of 5 MHz and 1 MHz, switching the rear panel select switch to 5 MHz and 1 MHz, respectively.

9.10.4.4 Set the rear panel select switch to "INT". Verify a 400 Hz square wave, 50% duty cycle at IC103, pin 13. Verify a 1 kHz square wave, 50% duty cycle at IC102, pin 13.

9.10.4.5 Set the instrument for internal AM 100%, 1 kHz. Verify a 50% duty cycle square wave at IC109, pin 3. Verify the absence of a signal at IC109, pin 8.

If necessary, adjust R114 "1 kHz Level Adjust" for a 20 Vpp sine wave at IC133, pin 7.

9.10.4.6 Set the instrument at 400 Hz, 100% AM modulation. Verify a 50% duty cycle square wave at IC109, pin 8. Verify the absence of a signal at IC109, pin 3. If necessary, adjust R15, "400 Hz Level Adjust" for 20 Vpp at IC133, pin 7.

9.10.4.7 Apply 1 Vpp sine wave at 1 kHz to the External Mod Jack J103. (Note J103 has a floating ground). Select EXT AM, 100% modulation. Check for visibly undistorted 20 Vpp sinewave at IC133, pin 1.

9.10.5 Perform the following tests to verify AM/Carrier Level circuitry:

9.10.5.1 Check for 10 $\pm$.03 VDC Reference at IC116, pin 6.

9.10.5.2 Select a Carrier frequency of 300.00000 MHz, internal 1 kHz, 100% Mod, Carrier level + 6 dBm, and RF on. Verify 12.08 Vpp $\pm$.5% centered at 6.04 VDC at IC132, pin 7. Verify 7.16

Vpp modulation sinewave centered at 3.58 VDC at J102, pin 3. Verify correct percentages of modulating voltage with respect to carrier level reference voltage at J102, pin 3 for the following modulation percentages: 90%, 50%, 30%, 10%, 0% or "MOD OFF".

9.10.5.3 With modulation of 100%, and RF on, vary carrier level from -7 dBm to +6 dBm in .1 dBm steps and verify that the modulation voltage swings between ground and 2x the DC carrier level reference voltage.

9.10.5.4 Select external AM, 100% modulation. Apply a 1 kHz 1 Vpp sinewave to the external modulation jack. Sweep the function generator from 10 Hz - 15 kHz. Verify that the modulation waveform is flat to within ±.5 dB with respect to the 1 kHz value.

9.10.5.5 Select internal AM, 100% modulation, 1 kHz modulation rate, and LVL +6 dBm. Using X1 scope probe apply output at J102, pin 3 to distortion analyzer. Verify that the total harmonic distortion does not exceed 1%.

9.10.5.6 Repeat step 9.10.5.5 using 400 Hz modulation rate.

9.10.6 The FM circuitry on the mainboard may be tested by performing the following procedures. Make certain there is an FM problem before proceeding with this section.

9.10.6.1 Connect a 2K, 1% resistor from J101, pin 3, to ground. Select internal FM, 1 MHz deviation, 1 kHz modulation rate, and a carrier frequency of 275.00000 MHz. Verify that no modulation waveform is present at the AM/LEVEL drive output IC140, pin 1. Verify that the voltage at IC126, pin 15, is 20 Vpp.

9.10.6.2 Record the binary number on the programming lines of Deviation Correction DAC IC126. Note that pins 12 and 13 (LSB) are hardwired to ground. Record the bits in the blank spaces of Table 9-5.

TABLE 9-5.
BINARY CORRECTION NUMBER

Bit	Pin of IC126	0 or 1	Weight
A1	4	___	10
A2	5	___	5
A3	6	___	2.5
A4	7	___	1.25
A5	8	___	.625
A6	9	___	.313
A7	10	___	.156
A8	11	___	.078
A9	12	0	N/A
A10	13	0	N/A

9.10.6.2.1 Add up the weights of the bits that are "1" and record the resulting voltage.

9.10.6.2.2 Note that these bits will remain the same until the circuitry is recalibrated or repaired. New values must be found at these times.

9.10.6.2.3 Verify the peak to peak voltage at IC134, pin 7 is within 2% of the voltage recorded in step 9.10.6.2.1, above.

9.10.6.3 Move the carrier frequency from 275-550 MHz with the spin knob while monitoring the voltage at IC134 pin 7. Voltage should vary as a function of carrier frequency. The exact manner of variance is determined by coarse tune data stored in memory, and need not be precisely measured at this stage of testing.

9.10.6.4 Return the carrier frequency to 275.00000 MHz. Measure and record the voltage at J101, pin 3.

NOTE: Make certain that the carrier frequency remains at 275.00000 MHz during the remainder of this procedure.

9.10.6.4.1 Change FM deviation to 100 kHz. The voltage at J101, pin 3 should be 1/10 that measured in step 9.10.6.4, above.

9.10.6.4.2 Change FM deviation to 50 kHz. The voltage at J101, pin 3 should be 1/20 that measured in step 9.10.6.4, above.

9.10.6.4.3 Change FM deviation to 5 kHz. The voltage at J101, pin 3 should be 1/200 that measured in step 9.10.6.4, above.

9.10.6.5 Select external FM and 1 MHz deviation. Apply a 1 kHz, 1 Vpp sine-wave to the External Mod Jack. Using an X1 probe, connect the output of J101, pin 3 to a distortion analyzer. Verify that total harmonic distortion is less than 1%.

9.10.7 Perform the following procedures to test the Direct Digital Synthesis circuitry on the Main Board. Make certain there is a DDS problem before proceeding with this section.

9.10.7.1 Set the Carrier frequency to 300.00000 MHz with any combination of RF Level and Modulation.

9.10.7.2 Verify the 1 MHz TTL reference at IC209, 210, 211 pin 11, and the inverted 1 MHz TTL square wave reference at IC213, pin 11.

9.10.7.3 Verify the 100.00 kHz sampled sine wave at IC215, pin 6 is like that in Figure 9-1, top trace.

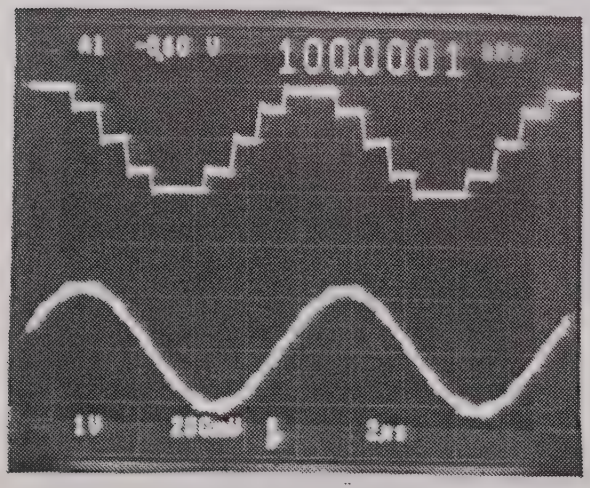


Figure 9-1. 100 kHz Sampled Sine Waves

9.10.7.4 Verify the 100.00 kHz .450 Vpp ±.0025 V Lowpass filtered sine-wave at IC217, pin 6 is like that of Figure 9-1, lower trace.

9.10.7.5 Verify the 100.00 kHz sine-wave output signals at IC219, pin 1 and pin 7, have amplitudes of .45 Vpp ±.05 Vpp. Voltage levels must not differ by more than ±.5%. Outputs should be sinusoidal and free from visible glitches. See Figure 9-2.

9.10.7.6 Check the quadrature relationship of the DDS outputs by using the oscilloscope. By measuring the time difference between corresponding points on the quadrature outputs, the phase relationship can be calculated if the output frequency is known. Be sure to use matched, properly compensated probes. Verify that the DDS output phase relationship is 90° ±3°. See Figure 9-2.

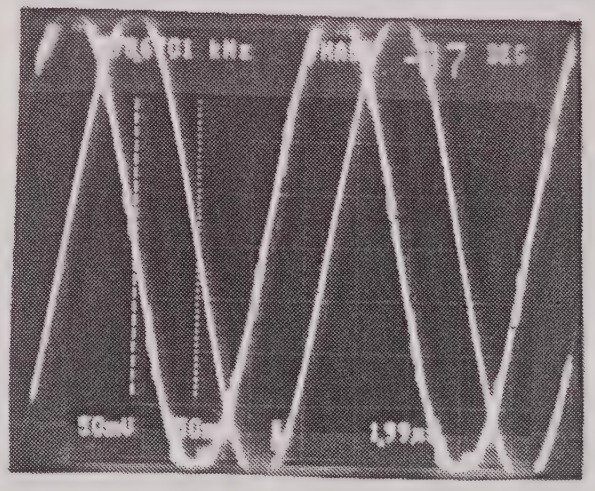


Figure 9-2. DDS Quadrature Outputs

9.10.7.7 Repeat steps 9.10.7.3 through 9.10.7.6 for the following carrier frequencies:

CARRIER FREQ	DDS FREQ
XXX.05000 MHz	150.00 kHz
XXX.09999 MHz	199.99 kHz

Note that at the maximum DDS frequency of 199.99 kHz (see Figure 9-3), normal deterministic phase jitter is present. Figure 9-3 is the same as Figure 9-1 except for the phase jitter at the higher frequency.

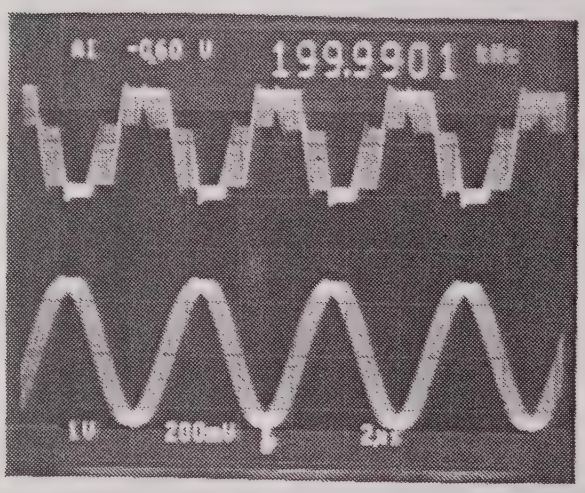


Figure 9-3. 199.99 kHz
Sampled Sine Waves

9.10.7.8 Use the instrument spin knob to move the DDS frequency in 10 Hz, 100 Hz, 1 kHz and 10 kHz steps. Verify correct DDS output frequencies at IC217, pin 6.

9.10.8 The L.O. Divider may be tested by the following procedure.

9.10.8.1 Set a signal generator to 500.0000 MHz, 0 dBm, Modulation OFF. Connect the signal generator to J402, the Local oscillator input.

9.10.8.2 Observe the prescaler output IC415, pin 11, for a TTL Level, 50 MHz square wave (50% duty cycle). See Figure 9-4, the top trace.

9.10.8.3 Observe the 5 MHz pulse output at IC416, pin 11. Refer to Figure 9-4, the lower trace.

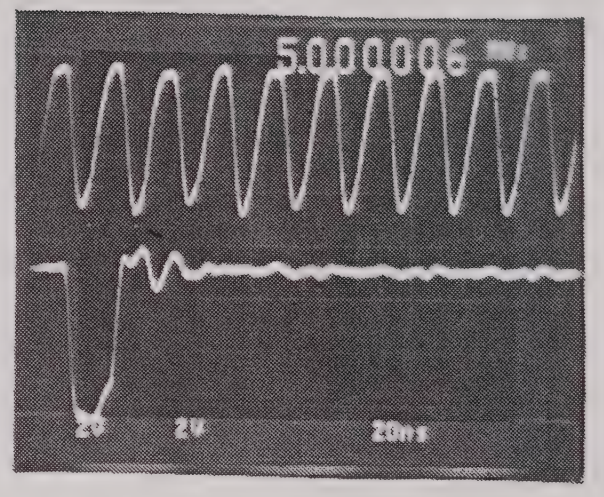


Figure 9-4. L.O. Divider Output,
50 MHz and 5 MHz Outputs

9.10.8.4 Observe the L.O. divider 1 MHz output at IC417, pin 7. Refer to the top trace of Figure 9-5. (The bottom trace of Figure 9-5 is the 1 MHz system difference, for comparison.)

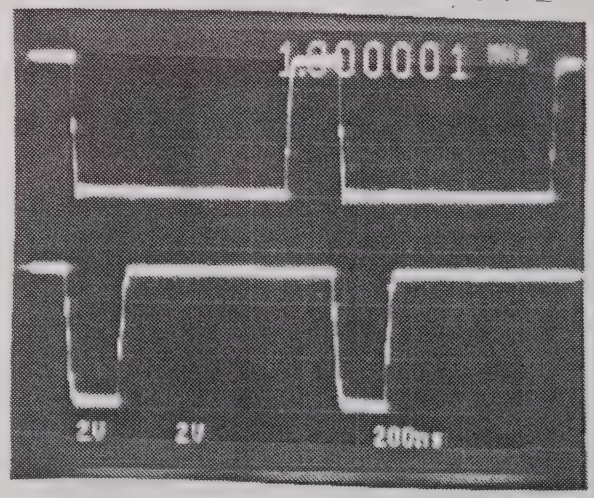


Figure 9-5. L.O. Divider 1 MHz

9.10.9 The Main Loop Fractional Divider on the Main Board may be tested using the following procedure.

9.10.9.1 Set the instrument frequency to 550.00000 MHz.

9.10.9.2 Apply a signal generator output to J401. Set the generator output level to +10 dBm at the same frequency as the instrument.

9.10.9.3 Check for proper divider operation by observing the pulse stretcher TTL waveform at IC423, pin 6. See Figure 9-6, the upper trace. Verify that the pulse width is $\geq$ 100 ns.

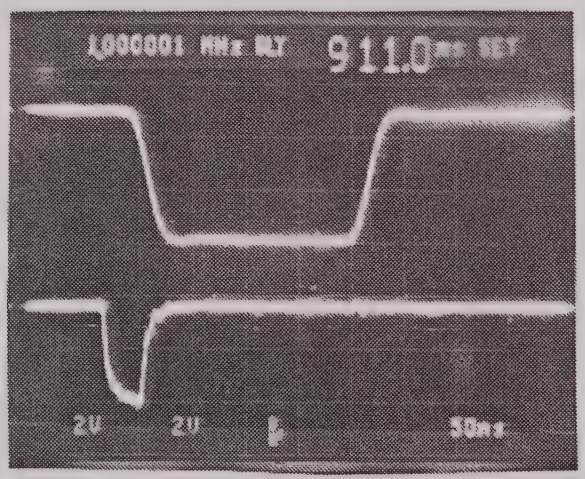


Figure 9-6. Pulse Stretch Output and ECL/TTL Translator Drive Pulse

9.10.9.4 Check the differential ECL/TTL translator drive to the pulse stretcher at IC421, pin 13. Refer to Figure 9-6, the lower trace. Signal must reliably cross the TTL threshold level (> 2.5 VDC).

9.10.9.5 Check IC401, pin 8 vs pin 3 to check ÷10/11 counter output signal (pin 8) and Modulus control waveform (pin 3) are of acceptable shape. See Figure 9-7. Do not use IC test clips.

9.10.9.6 Check the divider output frequency by connecting a scope probe to the frequency counter and measuring the frequency at the pulse stretcher output IC423, pin 6. Frequency should be 1 MHz with an error not to exceed the sum of the specified errors inherent in the signal generator and frequency counter time bases.

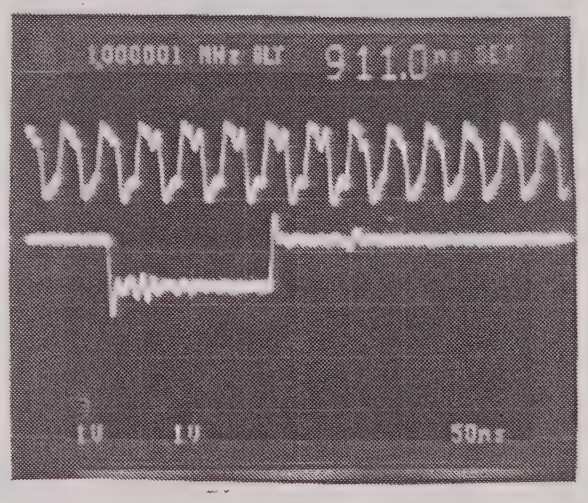


Figure 9-7. Divide-by-10/11 Output Signal (top trace) and Modulus Control Line

9.10.9.7 Vary the frequency from 275 to 550 MHz in 100 MHz, 10 MHz, and 1 MHz steps. Verify correct 1 MHz divider output at all frequencies.

9.10.9.8 Set the instrument and the signal generator frequencies to 550.00000 MHz. Reduce the signal generator output to +7 dBm. Verify that the divider output waveform and frequency as measured at the pulse stretcher output (IC423, pin 6), remain stable at 1 MHz.

9.10.9.9 Set the instrument and signal generator frequencies to 275.60000 MHz. Verify correct 1 MHz divider output as before. Check the "Fraction Control Clock" at IC406, pin 2, vs "N/N+1 Control" line at IC409, pin 6. See Figure 9-8. Note that a glitch on the "N/N+1 is normal.

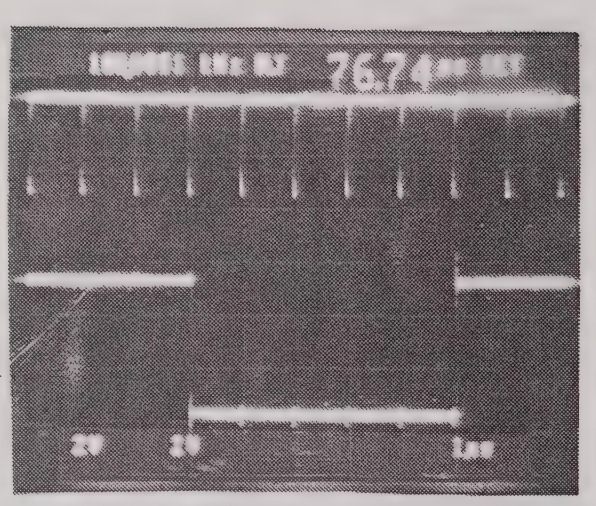


Figure 9-8. "Fraction Control Clock" (top trace) and "N/N+1 Control" Line

9.10.9.10 Vary the instrument and the test generator frequencies from 275.00000 MHz to 276.00000 MHz in 100 kHz increments, checking correct divider output frequency and "fraction control clock" waveform at each frequency.

9.10.10 Perform the follow tests to verify the ATTENUATOR CONTROL.

9.10.10.1 Set the instrument RF Level to +13 dBm, RF on, with any combination of carrier frequency and modulation. Move the cursor on the RF Level display to the 1 dB position.

9.10.10.2 Using the instrument's spin knob, reduce the RF Level in 1 dB steps. 10 dB of attenuation should switch in at a carrier level of -8 dBm. Verify correct attenuator control by checking for presence of 12 VDC on the first of the 10 dB pad section control feed-through capacitors.

9.10.10.3 Continue to reduce the RF Level in 1 dB steps, verifying that the attenuation increases in 10 dB increments at the appropriate points. The correct attenuator program should be verified by measurement of the attenuator drive voltages. Maximum attenuation is 130 dB.

9.10.10.4 Turn RF off. Verify all pads are energized, and relay opens.

9.10.11 The reverse power protection circuitry on the main board (see Section 8.5.2.5) will turn the RF power off if the breaker in the Programmable Attenuator trips. The breaker will trip if a voltage between 0.61 and 0.67 volts is detected by the attenuator's reverse power detector (see Section 8.2.15). This voltage may be monitored at pin 8 of P103 on the main board.

9.11 AMPLIFIER ASSEMBLY

The Amplifier Assembly Frequency Conversion circuitry and Leveler circuitry are described in detail in Sections 8.5.10 and 8.5.11, respectively, of this manual. Review these sections carefully. Troubleshooting the Amplifier Assembly is a straight forward procedure.

9.11.1 Check the input and output of each band in a frequency conversion network to isolate a problem. Obviously if no band works (for example, if bands H1, H2, and H3 of the doubler network are inoperative) the problem is common to each band.

9.11.2 When a failed network has been isolated, the problem will usually be a failed component.

9.11.3 Amplifier assembly transistor biasing for frequency conversion and leveler circuitry should be as shown in Table 9-6.

9.11.4 The L-band and H-band signal paths through the frequency conversion circuits of the amplifier assembly are controlled by band switching diodes. If the correct diodes are not turned on, the output signal will not be correct. The band switch/diode relationships are shown in Table 9-7.

TABLE 9-6.
AMPLIFIER ASSEMBLY TRANSISTOR BIASING

Transistor	Base	Collector
G.C.E.N Q601	1.4 V	7.6 V
L_1 Q606	.7 V	7.6 V
L_1 Q608	.8 V	7.4 V
Q700	.9 V	5.2 V
Q701	1.1 V	5.1 V
Q702	1.1 V	8.0 V
Q704	1.8 V	8.0 V
Q706	1.7 V	14.5 V

TABLE 9-7.
BANDSWITCH/DIODE RELATIONSHIPS

Band	Diodes Turned On
L_1	CR619, CR623, CR618, CR609, CR600, CR610
L_2	CR600, CR612, CR614, CR616, CR617, CR609
L_3	CR600, CR612, CR613, CR615, CR617, CR609
L_4	CR600, CR611, CR625, CR622, CR618, CR609
H_1	CR6C1, CR603, CR607, CR608
H_2	CR601, CR604, CR621, CR608
H_3	CR601, CR605, CR606, CR608

9.11.5 Course level control is performed by PIN diodes CR701 and CR702 which are driven through transistors Q709 and Q707 by the AM/Level drive at pin 3 of J603. Fine level control is performed by PIN diodes CR703 and CR704 which are driven by Q708 as part of the feedback system detailed in Section 8.5.11.2 of this manual.

9.11.6 When replacing components on the amplifier board it is very important to observe the following cautions:

9.11.6.1 The amplifier board, like all printed circuit boards found in this instrument, uses surface mount technology. DO NOT TWIST OR FLEX A CIRCUIT BOARD AS IT IS REMOVED/REPLACED BECAUSE THESE MOTIONS CAN DAMAGE SURFACE MOUNT DEVICES. LIFT ALL BOARDS DIRECTLY OUT OF THE INSTRUMENT TO REMOVE THEM. DO NOT "ROCK" A BOARD BACK AND FORTH TO LOOSEN IT.

9.11.6.2 The air coils found on the amplifier board are factory tuned and almost never need recalibration under normal operating conditions. They may be extremely difficult to recalibrate in the field if accidentally moved during repair work. BE VERY CAREFUL TO AVOID DISTURBING THE AIR COILS ON THE AMPLIFIER BOARD AT ANY TIME.

9.11.7 Perform the following steps to disassemble the amplifier assembly and remove the amplifier circuit board.

9.11.7.1 Remove power (unplug unit). Turn the unit on its back. Remove the bottom cover and the bottom shield just inside the bottom cover (see Figure 8-4). The GPIB and microprocessor boards will be exposed. The edges of the main board will be seen below the GPIB and microprocessor boards. The casting for the amplifier assembly (and oscillator assembly) is under the main board.

9.11.7.2 Remove the microprocessor board.

9.11.7.3 Remove the ten screws around the periphery of the main board that secure the main board to the amplifier assembly casting.

9.11.7.4 Lay the unit on its right side. Remove the left side handle and trim panel assemblies.

9.11.7.5 Remove the screws that secure the amplifier assembly to the left side panel.

9.11.7.6 Turn the instrument right side up. Remove the top cover.

9.11.7.7 Remove the three semi-rigid coax cables from the amplifier assembly (see Figure 8-2).

9.11.7.8 Remove the output cable from the programmable attenuator. Remove the attenuator.

9.11.7.9 Remove the screws that secure the amplifier assembly to the instrument chassis.

9.11.7.10 Remove the amplifier assembly by pulling up evenly at each end of the assembly. DO NOT "ROCK" THE ASSEMBLY BACK AND FORTH AS IT IS REMOVED. THERE IS A 20 PIN CONNECTOR BETWEEN THE AMPLIFIER ASSEMBLY AND THE MAIN BOARD THAT MAY BE DAMAGED IF THE AMPLIFIER ASSEMBLY IS NOT PULLED STRAIGHT OUT FROM THE CHASSIS.

9.11.7.11 Turn the amplifier assembly upside down and remove the nuts that secure the output transistor heat sinks to the underside of the amplifier assembly casting. Remove the heat sinks.

9.11.7.12 Turn the assembly right side up. Remove the screws that secure the lid to the amplifier assembly. Remove the lid.

9.11.7.13 Unsolder the SMA coax connector center pins from the amplifier circuit board.

9.11.7.14 Remove the allen set screws that secure the SMA coax connectors into the casting wall; these set screws are located in the top surface of the wall directly above each connector.

9.11.7.15 Remove the connector nuts which secure the SMA connectors to the wall casting. Carefully unscrew each connector out of the wall.

9.11.7.16 Remove the mounting screws that secure the amplifier circuit board from around the edge of the circuit board.

9.11.7.17 Grasp the circuit board shield at each end of the circuit board and carefully lift the board directly out. The connector described in Section 9.11.7.10, above, is also part of the amplifier board to assembly casting connection. This part of the connector may be damaged if the board is not removed with a uniform, even force. DO NOT "ROCK" THE BOARD TO LOOSEN IT. DO NOT TWIST THE BOARD IN ANY FASHION. (SEE SECTIONS 9.11.6.1 and 9.11.7.10.)

9.11.7.18 The amplifier board and amplifier assembly are reinstalled by reversing the procedures detailed above. Be careful to align the 20 pin connector to mate effortlessly as the board and assembly are reinstalled.

9.12 OSCILLATOR ASSEMBLY

The oscillator assembly contains an oscillator circuit board and a local oscillator circuit board. Circuitry found in the oscillator assembly is described in detail in Sections 8.5.7 (Main Lock and VCO), 8.5.8 (Leveler and Local Oscillator Lock), and 8.5.9 (Local Oscillator Board) of this manual. Review these sections carefully before troubleshooting the oscillator assembly.

9.12.1 The oscillator board VCO group oscillators cover the following frequency ranges:

Oscillator	Range
1	275 - 327 MHz
2	327 - 389 MHz
3	389 - 463 MHz
4	463 - 550 MHz

Isolating a problem to a specific range automatically simplifies the problem.

9.12.2 Switch IC501 selects which of the VCO oscillators is enabled. A failure in IC501 may result in the absence of one or more VCO ranges. To verify the switch is functional, monitor the voltage on the appropriate pin of IC501. The voltage should be -12.3 ±1 volt when its associated oscillator is on and greater than -1 volt when its associated oscillator is off.

9.12.3 If the entire VCO frequency (275-550 MHz) is inoperative, the problem may be a device common to each

oscillator circuit. Switch IC501, described above, is common to each oscillator circuit. The varactor drive to each oscillator comes from pin 1 of IC503B, another device common to the VCO group circuitry.

9.12.3.1 The varactor voltage range should be within 2-13 volts for each VCO group oscillator across its frequency range. Oscillator #3, for example should cover the frequency range from 389-463 MHz with a varactor voltage from 2-13 volts.

9.12.3.2 The voltage on pin 7 of IC514 should be between 0.5 - 4 volts throughout each range.

9.12.4 FM is added to the varactor drive by switch IC507 (see Section 8.5.7.6).

9.12.5 If there is a leveler problem, check RF detector CR533, DC Amplifier IC514B, and Diode Attenuator CR531.

9.12.6 If there is a problem with the RF to the Main Loop Divider, check transistors Q506, Q507, and Q514. These amplify the RF.

9.12.7 Transistors Q511 and Q512 provide bias for Oscillator Q508 on the Local Oscillator Board.

9.12.7.1 The emitter of Q512 should be -15.9 ±1 volt when the Local Oscillator (L.O.) is on. This voltage should be greater than -1 volt when the L.O. is off.

9.12.7.2 If there is a problem with the 500 MHz to the amplifier board, check the collector of Q509. The collector voltage should be between 3.8 and 9.8 volts. (A voltage greater than 8.5 volts <u>may</u> generate harmonic problems).

9.12.7.3 If there is a problem with the 500 MHz to the divide-by-500 Local Oscillator Divider Network, check the collector of Q510. The collector voltage should be between 3.8 and 9.8 volts. (A voltage greater than 8.5 volts <u>may</u> generate harmonic problems.)

9.12.7.4 If there is a problem with both 500 MHz trains described in Sections 9.12.7.2 and 9.12.7.3, above, check bias transistors Q511 and Q512 and check the oscillator itself (Q508).

9.12.8 Failures in oscillator assembly circuitry will typically be failed components. Verify the following transistor collector voltages:

<u>Transistor</u>	<u>Voltage</u>
Q505	6 ±.25 volts
Q506	3.8 - 9.8 volts
Q507	8 ±1 volts

Note that if the collector of Q506 is greater than 8.5 volts, harmonic problems <u>may</u> arise.

9.12.9 Power supply and reference voltages may be checked as follows:

<u>Location</u>	<u>Voltage</u>
IC504 pin 4	+15 V ±.75 V
pin 11	-15 V ±.75 V
IC502 pin 14	+5 V ±.5 V
IC505 pin 6	+10 V ±.1 V

9.12.10 When replacing components on the oscillator or local oscillator boards, it is very important to observe the following cautions:

9.12.10.1 These boards, like all printed circuit boards found in this instrument, use surface mount technology. DO NOT TWIST OR FLEX A CIRCUIT BOARD BECAUSE THESE MOTIONS MAY DAMAGE SURFACE MOUNT DEVICES.

9.12.10.2 The air coils found on these boards are factory tuned and almost never need recalibration under normal operating conditions. They may be extremely difficult to recalibrate in the field if accidentally moved during repair work. DO NOT DISTURB THE AIR COILS ON THESE BOARDS AT ANY TIME.

9.12.11 The oscillator and the local oscillator circuit boards sit inside a metal casting enclosure. Perform the following steps to access these boards.

9.12.11.1 Remove power (unplug unit). Remove the top cover.

9.12.11.2 Remove the output cable from the programmable attenuator (see Figure 8-2) to the RF output. Remove the coax cable from the oscillator assembly to the amplifier assembly.

9.12.11.3 Remove the screws securing the oscillator assembly protective lid to its casting enclosure. Remove the lid. The oscillator board and local oscillator board will be exposed; the oscillator board is the larger board located nearer the front panel.

9.12.11.4 It is not necessary to completely remove either board to perform repair/troubleshooting work. These boards are hinged together by wires that are soldered through five feed-throughs. When the appropriate connectors and securing screws have been removed (Sections 9.12.11.5 through 9.12.11.8), either board may be pivoted upward at this hinge. Be aware that the interconnecting wiring may break with excessive bending.

9.12.11.5 To free either board, first unsolder the SMA coax center connector pins from the appropriate circuit board.

9.12.11.6 Remove the allen set screws that secure the SMA coax connectors into the casting wall; these set screws are located in the top surface of the wall directly above each connector.

9.12.11.7 Remove the connector nuts which secure the SMA connectors to the wall casting. Carefully unscrew each connector out of the wall.

9.12.11.8 Remove the mounting screws that secure the circuit board from around the edge of the circuit board. The circuit board can now be pivoted into position.

9.12.11.9 Reverse the procedures detailed above to remount the oscillator assembly circuit boards and replace the instrument's protective covers.

SECTION 10

REFERENCE DRAWINGS AND REPLACEABLE PARTS

10.1 INTRODUCTION

This section contains the reference drawings (schematic, parts layout, and assembly) for the Model 2500.

The schematics are numbered from Figure 10-1 to Figure 10-15. More than one schematic may be used to clearly show detailed circuitry. For example, the Main Board requires four (4) schematics (Figures 10-2 through 10-5). The parts layout drawing is shown on the page facing its associated schematic. If a series of schematics is used, the parts layout will be shown opposite the first schematic in the series. The layout drawing for the Main Board, for example, is shown opposite Figure 10-2, the first of the four Main Board schematics. A schematic may show components found on several subassemblies. When this occurs, more than one parts layout may be required to clearly show detail. For example, the DPS-2F power supply requires three (3) layout drawings (Figures 10-6A, 10-6B, and 10-6C). Layout drawings have the same numeric designator as their associated schematics but also contain a letter suffix. A particular assembly may require more than one drawing to clearly show parts layout. In this case an additional numeric suffix is added. For example, Figure 10-8A1 and 10-8A2 show sides 1 and 2 of the Oscillator Board.

Assembly drawings are shown in Figures 10-16 through 10-23. Each assembly drawing refers to a "Reference BOM" (Bill of Material). Each BOM is included in Section 10 of this manual as a "Parts List". The references on the last two assembly drawings refer to Parts Lists present in Section 10 for the Oscillator Assembly (1110-00-2220, 1218-00-2290, and 1219-00-0629) and the Amplifier Board Frequency Conversion Section (1110-00-2230, 1218-00-2300, 1219-00-0630, and 1219-00-0611), respectively. A complete assembly drawing may require more than one figure. For example Figures 10-16A and 10-16B detail one view of the Model 2500 (and are listed as Figure 10-16A/B, Wrap-Up Kit, 2500).

Schematic abbreviations and other notes related to schematics are shown in Section 10.2 of this manual.

10.2 SCHEMATIC NOTES

The following notes and abbreviations pertain to all schematics. Additional notes pertaining to specific schematics are included on each schematic if required.

Unless otherwise noted, resistor values are given in ohms, capacitor values are given in pF, and inductor values are given in μH.

Denotes DC voltage reading in volts unless otherwise specified.

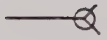
Denotes high impedance crystal detector reading in volts unless otherwise specified.

Denotes 50 ohm crystal detector reading in volts unless otherwise specified.

Signal or voltage source.

Connects to indicated signal or voltage source.

Arrow indicates clockwise rotation of wiper.



Coaxial jack

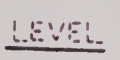
Coaxial plug

Coaxial cable

Factory adjusted part.

Denotes a front-panel device.

Denotes a rear-panel device.



Denotes a PC board adjustment or accessible module adjustment.

Denotes an internal module adjustment not accessible without removing module cover.

10.3 ORDER OF REFERENCE DRAWINGS

The reference drawings are located in the following order:

Figure 10-1	Schematic, Chassis Wiring (0014-30-0369)
Figure 10-2	Schematic, Mod Source/Ref Freq (Main Board; Sheet 1 of 4) (0014-30-0348)
Figure 10-2A	Parts Layout (Top Assembly Dwg), Main Board (0012-30-0016)
Figure 10-3	Schematic, Mod/Carrier Level (Main Board; Sheet 2 of 4) (0014-30-0348)
Figure 10-4	Schematic, Freq Div/Control (Main Board; Sheet 3 of 4) (0014-30-0348)
Figure 10-5	Schematic, Digital Synthesis (Main Board; Sheet 4 of 4) (0014-30-0348)
Parts List	Main Bd Assy, 2500 (1110-00-2240); Pages 1 thru 6
Figure 10-6	Schematic, DPS-2F (Power Supply) (0014-30-0365)
Parts List	P.C. Board Assy, 2500 (1218-00-2510); Pages 1 thru 2
Figure 10-6A1	Parts Layout, DPS-2F (0012-30-0027; Sheet 1 of 2)
Figure 10-6A2	Parts Layout, DPS-2F (0012-30-0027; Sheet 2 of 2)
Parts List	Power Supply, DPS2F, 2500 (1115-00-0045); Pages 1 thru 2
Figure 10-6B	Parts Layout, 2500 Power Supply Bd (0012-20-0031)
Parts List	PC Assy, DPS2F, 2500 (1118-00-0171); Page 1
Figure 10-6C	Parts Layout, Heatsink Assy (0012-20-0039)
Parts List	Heatsink Assy, DPS2F (1216-00-0274); Page 1
Figure 10-7	Schematic, Microprocessor Board (0014-30-0349)
Parts List	Uproc Bd Assy, 2500 (1110-00-2250); Pages 1 thru 2
Figure 10-7A	Parts Layout (Top Assy Dwg) Microprocessor Bd (0012-30-0020)

Figure 10-8	Schematic, Oscillator Board Main Lock and VCO Section (Sheet 1 of 2) (0014-30-0355)
Parts List	Oscillator Bd, 2500 (1218-00-2290); Pages 1 thru 2
Figure 10-8A1	Parts Layout, Oscillator Board (0012-20-0052; Side 1)
Figure 10-8A2	Parts Layout, Oscillator Board (0012-20-0052; Side 2)
Parts List	Hybrid PT KT, Osc Bd, 2500 (1219-00-0629); Pages 1 thru 3
Figure 10-9	Schematic, Oscillator Board Leveler & L.O. Lock Section (Sheet 2 of 2) (0014-30-0355)
Figure 10-10	Schematic, Local Oscillator Board (0014-30-0371)
Parts List	Local Osc Bd, 2500 (1218-00-2590); Page 1
Figure 10-10A	Parts Layout (Top Assy Dwg) Local Oscillator Bd (0012-20-0051)
Parts List	Hybrid PTS KT, Local Osc Bd, 2500 (1219-00-0631); Page 1
Figure 10-11	Schematic, Amp Board Freq. Conv. Section (Sheet 1 of 2) (0014-30-0363)
Figure 10-11A	Parts Layout, Amp Bd (0012-30-0035)
Parts List	Hybrid PT KT, Amp Bd, 2500 (1219-00-0630); Pages 1 thru 4
Figure 10-12	Schematic,Amp Board Leveler Section (Sheet 2 of 2) (0014-30-0363)
Parts List	Amplifier Bd, 2500 (1218-00-2300); Pages 1 thru 3
Figure 10-13	Schematic, Display Bd, (Sheet 1 of 2) (0014-30-0351)
Parts List	Display Bd, 2500 (1218-00-2280); Pages 1 thru 2
Figure 10-13A	Parts Layout (Top Assembly Dwg), Display Bd (0012-30-0017)
Figure 10-14	Schematic, Display Bd, (Sheet 2 of 2) (0014-30-0351)
Figure 10-15	Schematic, Keyboard (0014-30-0352)
Figure 10-15A	Parts Layout (Top Assembly Dwg), Keyboard (0012-30-0019)
Figures 10-16A/B	Assembly Dwgs - Wrap Up Kit (0012-30-0033)
Parts List	Wrap Up Kit, 2500 (1111-00-0179); Page 1
Figure 10-17	Assembly Dwg - Final Assy (0012-30-0022)
Parts List	Final Assy, 2500 (1111-00-0178); Page 1
Figure 10-18	Assembly Dwg - Chassis Assy (0012-30-0026)
Parts List	Chassis Assy, 2500 (1111-00-0185); Page 1
Figure 10-19	Assembly Dwg - Front Panel Mechanical Assy (0012-30-0030)
Parts List	FP Mechanical Assy, 2500 (1216-00-0224); Page 1
Figure 10-20	Assembly Dwg - Front Panel Assy (0012-30-0029)
Parts List	F Panel Assy, 2500 (1110-00-2210); Page 1
Figures 10-21A/B	Assembly Dwgs - Mid-Section Assy (0012-30-0023) (2 Sheets)
Parts List	Midsection Assy, 2500 (1110-00-2290); Page 1
Figure 10-22	Assembly Dwg - Oscillator Assy (0012-30-0024)
Parts List	Oscillator Assy, 2500 (1110-00-2220); Page 1
Figure 10-23	Assembly Dwg - Amplifier Assy (0012-30-0025)
Parts List	Amplifier Assy, 2500 (1110-00-2230); Page 1

11.1 INTRODUCTION

This section contains engineering updates and corrections of errors in the manual.

11.2 MANUAL CHANGES

Wavetek's product improvement program incorporates the latest electronic developments into these instruments as rapidly as development and testing permit. Due to the time required to document and print these instruction manuals, it is not always possible to include the changes in the original printing. Change information, if any, appears after this page.

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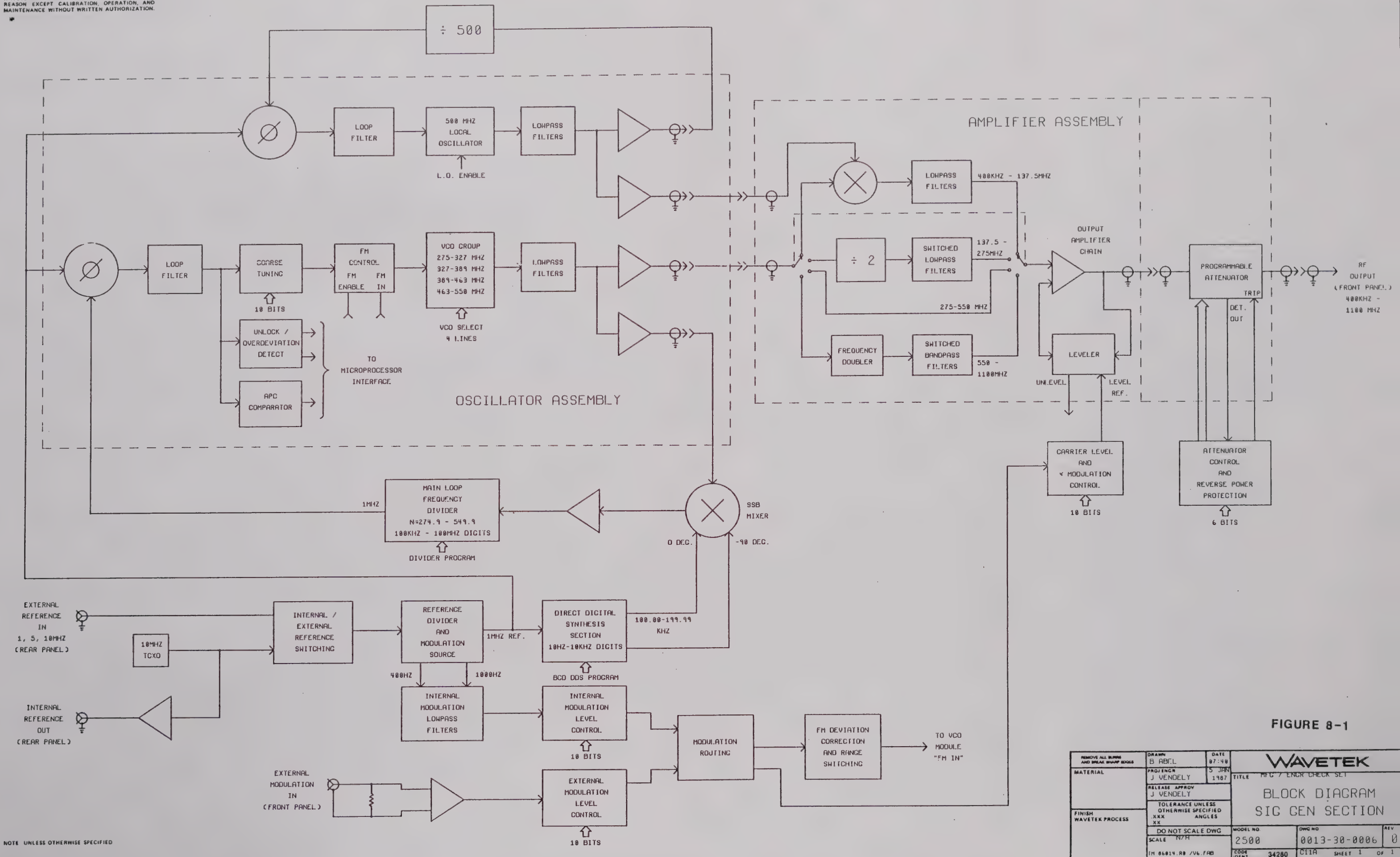

NOTE UNLESS OTHERWISE SPECIFIED

FIGURE 8-1

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B ABEL	DATE 07:48 5 JAN 1987	WAVETEK
MATERIAL	PROJ ENGR J VENDELY		TITLE MFG / ENGR CHECK SET
	RELEASE APPROV J VENDELY		BLOCK DIAGRAM SIG GEN SECTION
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG SCALE N/M	MODEL NO 2500	DWG NO 0013-30-0006 REV 0
	IM 86014.R0 /V6.FAB	CODE IDENT 34280	CIIA SHEET 1 OF 1

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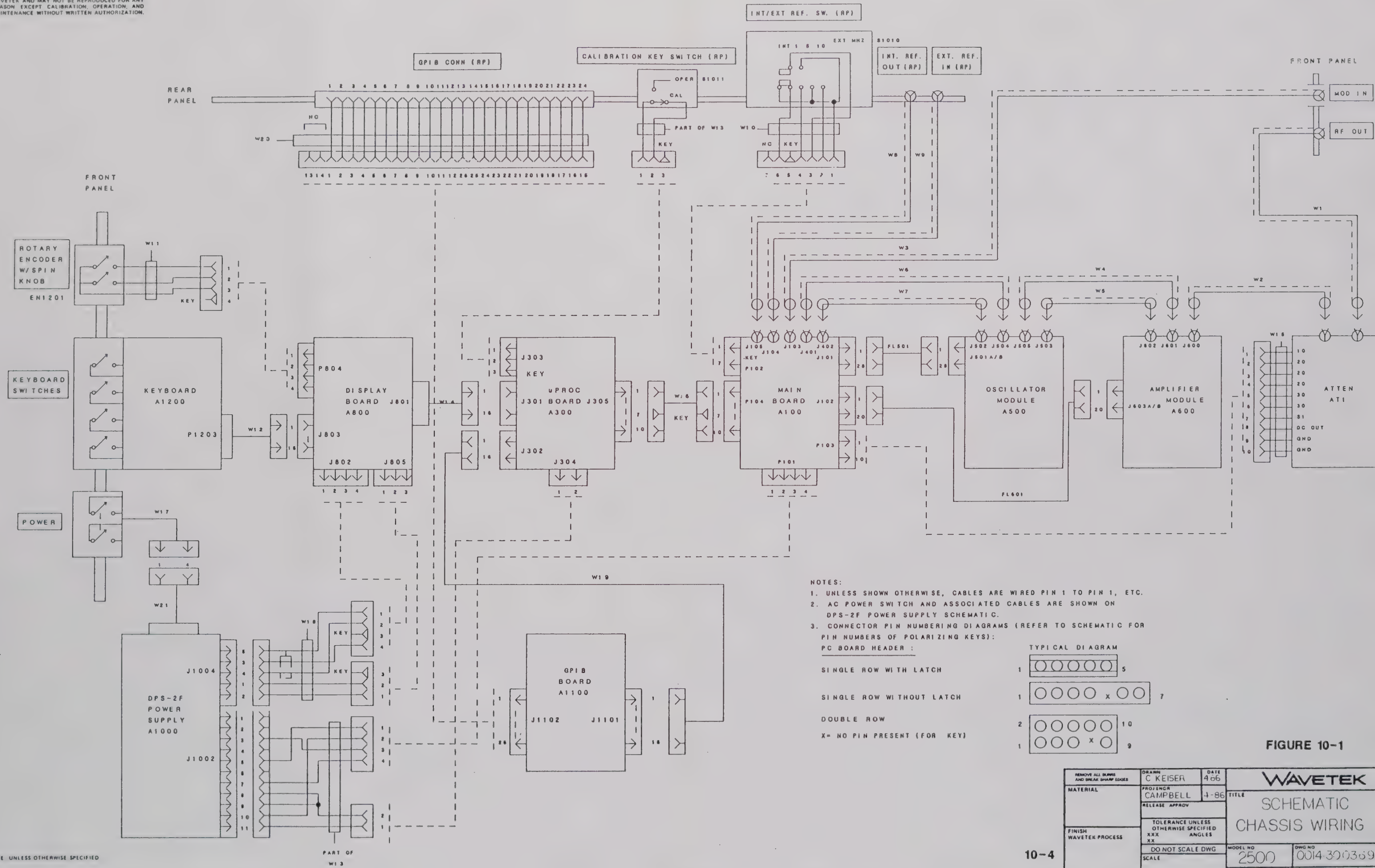
REV	ECN	BY	DATE
A	PIN 3662	CK	1



NOTES:
1. UNLESS SHOWN OTHERWISE, CABLES ARE WIRED PIN 1 TO PIN 1, ETC.
2. AC POWER SWITCH AND ASSOCIATED CABLES ARE SHOWN ON DPS-2F POWER SUPPLY SCHEMATIC.
3. CONNECTOR PIN NUMBERING DIAGRAMS (REFER TO SCHEMATIC FOR PIN NUMBERS OF POLARIZING KEYS):

PC BOARD HEADER :	TYPICAL DIAGRAM
SINGLE ROW WITH LATCH	1 ○○○○○ 5
SINGLE ROW WITHOUT LATCH	1 ○○○○ x ○○ 7
DOUBLE ROW	2 ○○○○○ 10
X= NO PIN PRESENT (FOR KEY)	1 ○○○ x ○ 9

FIGURE 10-1

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN C KEISER	DATE 4-86	WAVETEK
MATERIAL	PROJENGR CAMPBELL	4-86	TITLE SCHEMATIC CHASSIS WIRING
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG		MODEL NO 2500
	SCALE		DWG NO 0014-300369
			CODE IDENT 34280
			SHEET 1

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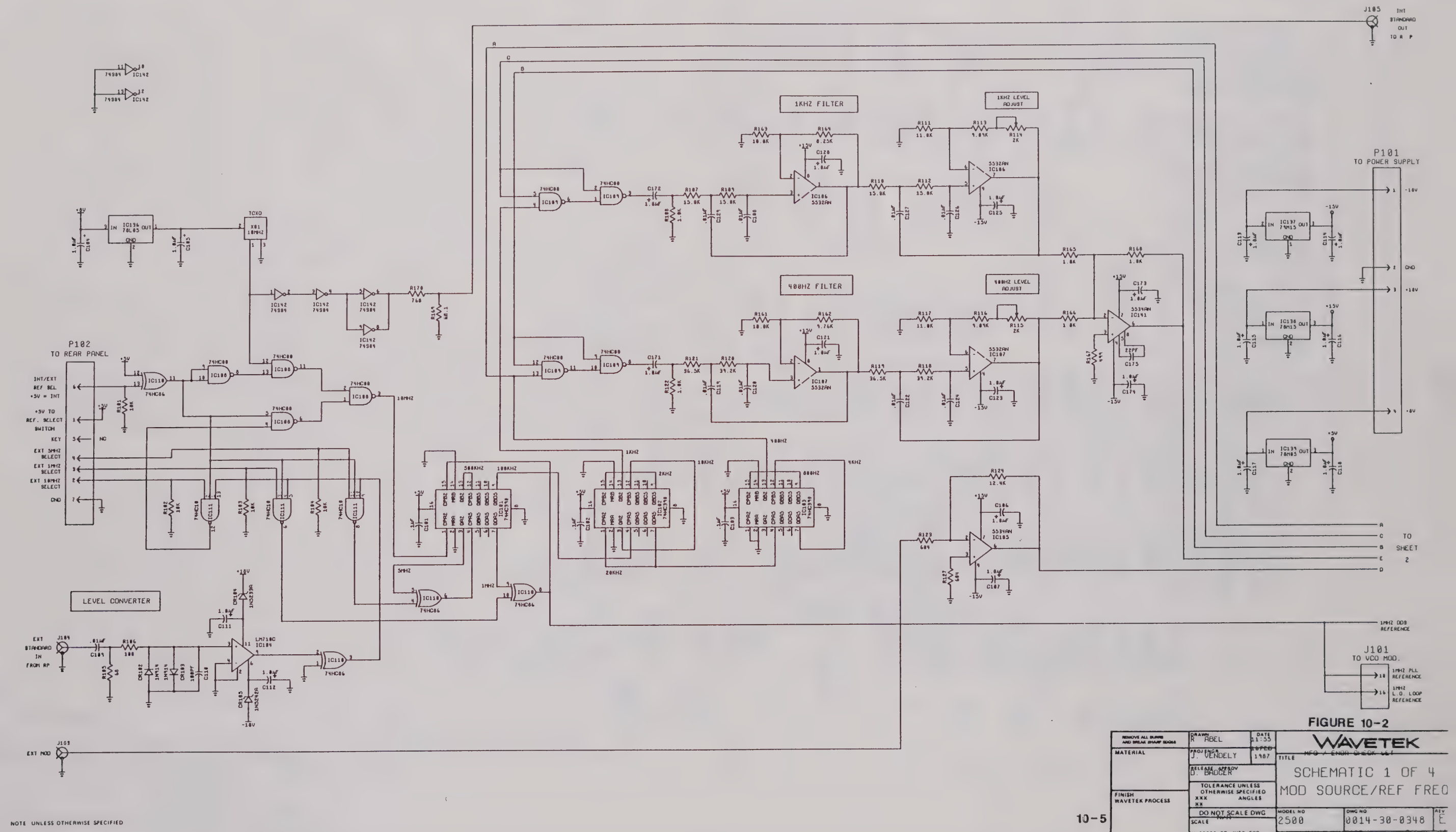

FIGURE 10-2

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R ABEL	DATE 11:55	WAVETEK
MATERIAL	PROJ ENGR J. VENDELY	19FEB 1987	TITLE SCHEMATIC 1 OF 4 MOD SOURCE/REF FREQ
FINISH WAVETEK PROCESS	RELEASE APPROV D. BADGER		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG SCALE N.A.T.	MODEL NO 2500	DWG NO 0014-30-0348 REV E
	M.85828.RB /V73./FAB	CODE IDENT 34280	SIZE A SHEET 1 OF 10

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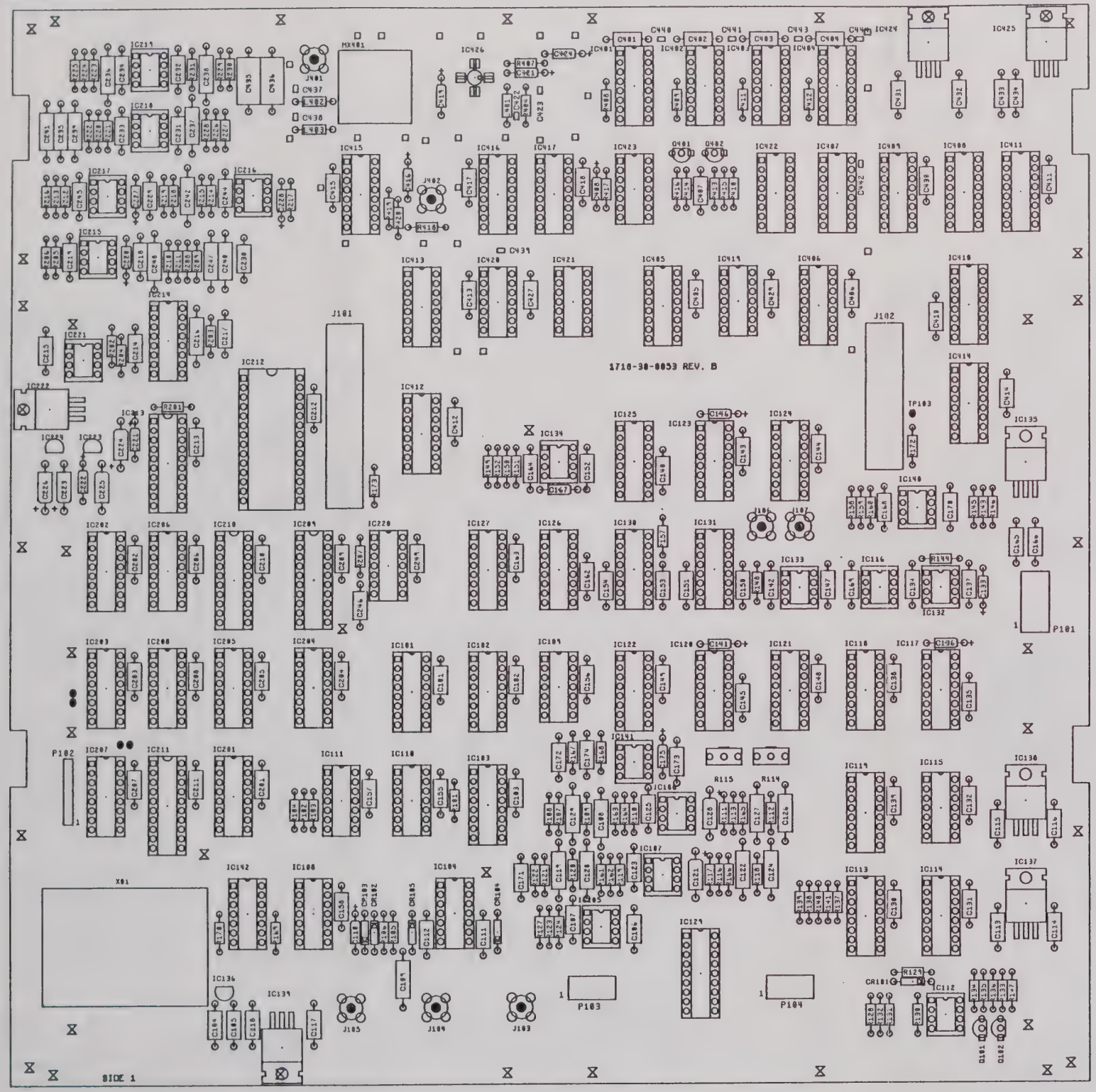

FIGURE 10-2A

REV	ECN	BY	DAT

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. ABEL	DATE 18:42 3 JAN 19[illegible]	WAVETEK
MATERIAL C-10 .062 DOUBLE SIDED	PROJENGR J. VENDELY		TITLE MFG / ENGR CHECK SET TOP ASSEMBLY D MAIN BOARD
	RELEASE APPROV D. BADGER		
FINISH WAVETEK PROCESS PTH T/L FINISH SOLDER BOTH LEGEND TOP	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG SCALE 1:1.5 TM.8582B.RB /V71.FAB	MODEL NO. 2500	DWG NO. 0012-30-001
		CODE IDENT 34280	C2H SHEET 3

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REV	ECN	BY	DATE	APP

LEVEL/AM

INTERNAL MODULATION

EXTERNAL MODULATION

DEVIATION CORRECTION

P104 TO µP BD.

P103

P103 TO ATTEN.

J102 TO RF MOD.

J101 TO VCO MOD.

J101 TO VCO MOD.

J102 TO RF MOD.

TO SHEET 1

REVERSE POWER DETECT FROM ATTEN.

IC135 78M15

IC129 UDN6118A

IC130 HI-201

IC131 HI-201

IC117 DAC1020LCN

IC120 DAC1020LCN

IC123 DAC1020LCN

IC126 DAC1020

IC132 LF412CN

IC133 TL082

IC134 5532

IC136 REF-01

IC112 CA3240

IC113 74HC259

IC114 CD4021

IC115 CD4070

IC116 74HC595

IC121 74HC595

IC122 74HC595

IC124 74HC595

IC125 74HC595

IC127 74HC595

IC140 TL082

Q101 2N3904

Q102 2N3904

CR101 1N914

J106

J107

SEE NOTE 1

CLOCK0
CLOCK1
CLOCK2
CLOCK3
CLOCK4
CLOCK6
STROBE
DATA

NOTES:

1. J106, J107 NOT INSTALLED ON STANDARD MODEL 2500 MAIN BD. LAND BETWEEN J106 & J107 IS SEPARARTED WHEN UNIT IS EQUIPPED WITH FSK MODULATOR.

FIGURE 10-3

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. ABEL	DATE 11:56	WAVETEK
MATERIAL	PROJ ENGR J. VENDELY	10/20 1987	TITLE SCHEMATIC 2 OF 4 MOD / CARRIER LEVEL
FINISH WAVETEK PROCESS	RELEASE APPROV D. BADGER		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG SCALE NONE	MODEL NO 2500	DWG NO 0014-30-0348 REV E
	M.85028 RB /V73 FAB	CODE IDENT 34280	SIZE A SHEET 0 OF 10

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REV	ECN	BY	D

÷ 10/11

1MHZ

10MHZ

100MHZ

PULSE STRETCHER

MODULUS CONTROL

FRAME COUNT

N/N+1 CONTROL

FRACTION CONTROL CLOCK

FRACTION COUNT

ADDER

1 MHZ DATA

100KHZ DATA

100KHZ DATA

100KHZ DATA

100KHZ DATA

CLOCK0

STROBE

DATA

CLOCK1

÷ 10

÷ 10

÷ 5

J101
TO VCO MOD.

1MHZ TO MAIN LOOP PHASE DET

1MHZ TO LO LOOP PHASE DET

L98

COARSE TUNE CONTROL

R98

B1
B2
B3
B4
LO ENABLE

VCO BANDSWITCHING

J102
TO RF MOD.

1GHZ BANDSWITCHING

FREQUENCY CONVERTER

L9 BANDSWITCHING

CC ENABLE

FIGURE 10-4

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B LABEL	DATE 16 FEB 1987	WAVETEK MFG / ENGR CHECK OFF
MATERIAL	PROVENCE J VENDELY		TITLE SCHEMATIC 3 OF FREQ DIV / CONTR
FINISH WAVETEK PROCESS	RELEASE APPROV D BADGER		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG	MODEL NO 2500	DWG NO 0014-30-0348
	SCALE m:85020.RB /V73.FRB	CODE IDENT 34280	SIZE A SHEET

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REV	ECN	BY	DATE	APP

PHASE ACCUMULATOR

MSD

LSD

SINE TABLE

250 KHZ LPF

PHASE SPLITTER

DATA

CLOCK

STROBE

IC201 74HC595 · IC202 74HC595 · IC203 74HC595 · IC204 74F583 · IC205 74F583 · IC206 74F583 · IC207 74F583 · IC208 74F583 · IC209 74HC273 · IC210 74HC273 · IC211 74HC273 · IC212 27C64 · IC213 74HC273 · IC214 DAC-80EQ · IC215 NE5534A · IC216 NE5534A · IC217 NE5534A · IC218 NE5532A · IC219 NE5532A · IC220 74HC86 · IC221 REF-01 · IC222 78M05 · IC223 78L15 · IC224 79L15

JUMPERS ADDED FOR MAIN BOARD UTILIZING THE F.S.K. MODULATOR.

CLOCK6

1MHZ DDS REFERENCE

OUT1 0 DEG.

OUT2 - 90 DEG.

100-199.999 KHZ QUADRATURE DRIVE TO SSB MIXER

* : NOTE IC201, IC202, IC203 WILL NOT BE INSTALLED ON UNITS MODIFIED WITH THE F.S.K. MODULATOR.

NOTE: UNLESS OTHERWISE SPECIFIED

FIGURE 10-5

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. ABEL	DATE 11-FEB 1987	WAVETEK
MATERIAL	PROJENGR B. SHM		TITLE SCHEMATIC 4 OF 4 DIGITAL SYNTHESIS
	RELEASE MFGRV D. BADGER		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG	MODEL NO. 2500	DWG NO 0014-30-0348 REV E
	SCALE N.05828.RB /V73.FAB	CODE IDENT 34280	SIZE A SHEET 1 OF 10

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
IC409	4-BIT BINARY ADDER WITH FAST CARRY STATIC SENSITIVE	MC74HC283	MOT	8007-42-8311	1.000
IC416	DECADE COUNTER,BCD STATIC SENSITIVE	74F162A	FCD	8007-41-6212	1.000
IC422	TRIPLE OR/NOR STATIC SENSITIVE	MC10105L	MOT	8001-01-0500	1.000
IC423	2-D TYP,POS EDG TRIG FLIP-FLOP W/CLR&PRE-SET,STATIC SENSITIVE	MC74HC74	MOT	8000-74-7403	1.000
IC426	UWAVE WB AMP,0204 STATIC SENSITIVE	MSA-0204	AVT	4902-00-2040	1.000
J101A J101B	MOD,RECEPT,PC MT,.1 CTR,14 PIN,TOP ENTRY FROM:2112-35-0011	2112-35-0013	W-I	2112-35-0013	2.000
J102A J102B	MOD RECEPT,PC MT,.1" CTR,10 PIN,TOP ENTRY FROM:2112-35-0010	2112-35-0012	W-I	2112-35-0012	2.000
J103 J104 J105 J401 J402	CONN,RF,STR,JACK	700209	CRLWV	2110-08-0006	5.000
KIT 1	EPROM KIT,MB,2500	1219-00-0614	W-I	1219-00-0614	1.000
KIT 2	MPWR KIT,MB,2500	1219-00-0618	W-I	1219-00-0618	1.000
L401	CHOKE,COATED,1UH,10% D=0.120IN,L=0.300IN, I=385MA	08N1R0	JEF	1810-03-0010	1.000
MX401	MIXER,275-550 MHZ STATIC SENSITIVE #2	CLP-A56;SSB MODULATOR	SYNRG	3010-54-0011	1.000
P101	PLUG,LKG,STRT,4-PIN	09-65-1041	MOL	2112-06-0001	1.000
P102	HEADER,7-PIN STRT REF:2112-07-0000	65501-407	BER	2112-07-0005	1.000
P103 P104	HDR,STRT,DBL,10-PIN REF:2112-07-0042	65611-110	BER	2112-07-0076	2.000
Q101 Q102	NPN,TO-92,GP AMP/SW F=300,V=40,Icex=50nA P=625mW,hFE=100,SS#2	2N3904	NAT	4901-03-9040	2.000
Q401 Q402	PNP,TO-92,GP AMP/SW F=300,V=40,Icex=50nA P=625mW,hFE=100,SS#2	2N3906	T-I	4901-03-9060	2.000
R101 R102 R103 R104 R134 R135 R136 R137 R138 R139 R140 R141 R147 R211	RES,C,1/4W,5%,10K	CF1/4-10K	ASE	4700-15-1002	14.000
R105 R407 R420	RES,C,1/4W,5%,68	CF1/4-68	ASE	4700-15-6809	3.000
R106	RES,C,1/4W,5%,100	CF1/4-100	ASE	4700-15-1000	1.000
R107 R109 R110 R112	RES,MF,1/8W,1%,15K	RN55D-15K	MILSP	4701-03-1502	4.000

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
R108 R122 R123 R126 R165 R166 R168 R205	RES,MF,1/8W,1%,1K	RN55D-1K	MILSP	4701-03-1001	8.000
R111 R117	RES,MF,1/8W,1%,11.0K	RN55D-11.0K	MILSP	4701-03-1102	2.000
R113 R116 R231	RES,MF,1/8W,1%,9.09K	RN55D-9.09K	MILSP	4701-03-9091	3.000
R114 R115	TRM,CR,1,2K,10%,PC 1T,PN,CW,.375H,.200W ,375L,SA	360S202B	CTS	4610-00-1202	2.000
R118 R120	RES,MF,1/8W,1%,39.2K	RN55D-39.2K	MILSP	4701-03-3922	2.000
R119 R121	RES,MF,1/8W,1%,36.5K TAPE AND REEL	RN55D-36.5K	MILSP	4701-03-3652	2.000
R124 R127	RES,MF,1/8W,1%,20.5K	RN55D-20.5K	MILSP	4701-03-2052	2.000
R125	RES,MF,1/8W,1%,845	RN55D-845	MILSP	4701-03-8450	1.000
R128	RES,C,1/4W,5%,1M	CF1/4-1M	ASE	4700-15-1004	1.000
R129	RES,C,1/4W,5%,1K	CF1/4-1K	ASE	4700-15-1001	1.000
R130	RES,1/8W,1%, 49.9K	RN55D-49.9K	MILSP	4701-03-4992	1.000
R131	RES,MF,1/8W,1%,13.0K	RN55D-13.0K	MILSP	4701-03-1302	1.000
R132	RES,MF,1/8W,1%,1.82K	RN55D-1.82K	MILSP	4701-03-1821	1.000
R133	RES,C,1/4W,5%,33K	CF1/4-33K	ASE	4700-15-3302	1.000
R143 R145 R149 R150 R151 R152 R158 R159 R161 R163 R204 R212 R213 R214 R215 R220 R221 R223 R224 R226 R227 R229 R230	RES,MF,1/8W,1%,10K	RN55D-10K	MILSP	4701-03-1002	23.000
R144	RES,MF,1/8W,6.04K	RN55D-6.04K	MILSP	4701-03-6041	1.000
R146	RES,MF,1/8W,1%,2.74K	RN55D-2.74K	MILSP	4701 03-2741	1.000
R148	RES,MF,1/8W,1%,182K	RN55D-182K	MILSP	4701-03-1823	1.000
R157	RES,MF,1/8W,1%,19.1K	RN55D-19.1K	MILSP	4701-03-1912	1.000
R160 R202 R203	RES,MF,1/8W,1%,4.99K	RN55D-4.99K	MILSP	4701-03-4991	3.000
R162	RES,MF,1/8W,1%,9.76K	RN55D-9.76K	MILSP	4701-03-9761	1.000
R164	RES,MF,1/8W,1%,8.25K	RN55D 8.25K	MILSP	4701-03-8253	1.000
R167	RES,MF,1/8W,1%,499	RN55D-499	MILSP	4701 03-4990	1.000
R169	RES,MF,1/8W,1%,68.1	RN55D-68.1	MILSP	4701-03-6819	1.000
R170	RES,MF,1/8W,1%,768	RN55D-768	MILSP	4701-03-7680	1.000
R172	RES,C,1/4W,5%,47	CF1/4-47	ASE	4700-15-4709	1.000
R173	RES,MF,1/8W,1%,95.3	RN55D-95.3	MILSP	4701-03-9539	1.000
R201 R207	RES,C,1/4W,5%,4.7K	CF1/4-4.7K	ASE	4700-15-4701	2.000

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
R206	RES,MF,1/8W,5%,680	RN55D-680	MILSP	4701-03-6800	1.000
R208	RES,MF,1/8W,1%,174	RN55D-174	MILSP	4701-03-1740	1.000
R209	RES,MF,1/8W,1%,3.01K	RN55D-3.01K	MILSP	4701-03-3011	1.000
R210	RES,C,1/4W,5%,3.3K	CF1/4-3.3K	ASE	4700-15-3301	1.000
R216	RES,MF,1/8W,1%,1.58K	RN55D-1.58K	MILSP	4701-03-1581	1.000
R217	RES,MF,1/8W,1%,619	RN55D-619	MILSP	4701-03-6190	1.000
R218	RES,MF,1/8W,1%,309	RN55D-309	MILSP	4701-03-3090	1.000
R219	RES,MF,1/8W,1%,1.43K	RN55D-1.43K	MILSP	4701-03-1431	1.000
R222	RES,MF,1/8W,1%,191	RN55D-191	MILSP	4701-03-1910	1.000
R225	RES,MF,1/8W,1%,2.21K	RN55D-2.21K	MILSP	4701-03-2211	1.000
R228	RES,MF,1/8W,1%,750	RN55D-750	MILSP	4701-03-7500	1.000
R403	RES,C,1/4W,5%,240	RCF-240-QB	CII	4700-15-2400	1.000
R404	RES,C,1/4W,5%,560	CF1/4-560	ASE	4700-15-5600	1.000
R408 R409 R410 R411 R412 R413 R414 R419	RES,C,1/4W,5%,470	CF1/4-470	ASE	4700-15-4700	8.000
R415	RES,C,1/4W,5%,62	CF1/4-62	ASE	4700-15-6209	1.000
R416 R418	RES,C,1/4W,5%,220	CF1/4-220	ASE	4700-15-2200	2.000
R417	RES,C,1/4W,5%,2K	CF1/4-2K	ASE	4700-15-2001	1.000
SCH	SCH,MAIN BD,2500	0014-30-0348	W-I	0014-30-0348	1.000
X01	TCXO-50-40, CRYSTAL OSCILLATOR TEMP COMP NORMED IN	TCXO-50-40	ISTMF	2311-00-0015	1.000

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
1	SHIELD 1 FOR MAIN BD PER B/P	1410-30-7800	W-I	1410-30-7800	1.000
2	SHIELD 2 FOR MAIN BD PER B/P	1410-30-7810	W-I	1410-30-7810	1.000
3	SHIELD 3 FOR MAIN BD PER B/P	1410-30-7820	W-I	1410-30-7820	1.000
4	COVER 1 FOR MAIN BD PER B/P	1410-30-7830	W-I	1410-30-7830	1.000
5	COVER 2 FOR MAIN BD PER B/P	1410-30-7840	W-I	1410-30-7840	1.000
6	COVER 3 FOR MAIN BD PER B/P	1410-30-7850	W-I	1410-30-7850	1.000
C101 C102 C103 C130 C131 C132 C134 C135 C137 C138 C139 C140 C142 C143 C144 C145 C147 C148 C149 C150 C151 C152 C153 C154 C155 C156 C157 C158 C162 C163 C164 C165 C166 C168 C169 C170 C201 C202 C203 C204 C205 C206 C207 C208 C209 C210 C211 C212 C213 C214 C215 C217 C218 C219 C229 C230 C231 C232 C233 C234 C244 C245 C246 C249 C401 C402 C403 C404 C405 C406 C407 C410 C411 C412 C413 C414 C415 C417 C418 C427 C429 C430	.1 MF 20%,50V,GENERL PURPOSE AXIAL LEAD TAPE AND REEL	SA205E1042AA	AVX	1510-17-1104	82.000
C104 C105 C106 C107 C111 C112 C113 C114 C115 C116 C117 C118 C121 C123 C125 C128 C171 C172 C173 C174 C221 C222 C431 C432 C433 C434	CAP,TANT,25V,1UF	100DE105K25A2	ACI	1510-21-7010	26.000
C108 C119 C120 C122 C124 C126 C127 C129 C216	CAP,POLY,50 VDC,.01, 2%TAPE AND REEL	RV2A103G	IMB	1510-64-6103	9.000
C109 C416 C421 C424	CAP,CER,.01UF,50V 10%,AXL,X7R .09"DX.16"L	592CX7R103K050B	SPR	1510-16-4103	4.000
C110 C408	CAP,CER,100V,100PF	C114G101J1G5CA	KEMET	1510-16-4101	2.000
C133 C136 C141 C146 C167	CAP,CER,200V,5.1 PF	C114G519C2G5CA	KEMET	1510-16-4519	5.000
C175 C220 C227 C228	CAP,CER,200V,22 PF	C114G220J2G5CA	KEMET	1510-16-4220	4.000
C223 C224 C225 C226	CAP,TANT,25V,10UF	100DE106M20C2	ACI	1510-21-7100	4.000
C235 C236 C237 C238 C239 C240 C241 C242	CAP,POLY,50 VDC,.001 2%TAPE AND REEL	RV2A102G	IMB	1510-64-6102	8.000
C247 C248	CAP,POLY,50VDC,.0047 2%	RV2A472G	IMB	1510-64-6472	2.000

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
C419 C420 C423	CAP,CER,50V,470	C114G471J5G5CA	KEMET	1510-16-4471	3.000
C435 C436	CAP,CER,50V,1.0 UF	C202C105K5R5LA	KEMET	1510-16-6105	2.000
CR101 CR102 CR103	DIODE,SIGNAL,GP AXIAL,V=75V,IO=10mA CT=4pF,SS#2	1N914	G-E	4807-01-0914	3.000
CR104	DIODE,ZENER,500mW,GP DO-35,V=6.0,IT=20mA +/-10%,SS#2	1N5233	MOT	4801-01-5233	1.000
CR105	DIODE,ZENER,1W,GP DO-41,V=12,IT=21mA IF=76mA,+/-5%,SS#2	1N4742A	MOT	4801-02-0063	1.000
IC101 IC102 IC103 IC417	DUAL 4-STAGE BINARY RIPPLE COUNTER STATIC SENSITIVE	MC74HC390	MOT	8007-43-9011	4.000
IC104	VOLTAGE COMPARATOR STATIC SENSITIVE #2	LM710CN	NAT	7000-07-1000	1.000
IC105 IC141 IC215 IC216 IC217	OP AMP,LOW NOISE PLAS,DIP-8,20Vdc 200KHz,13V/uS,SS#2	NE5534AN	SIG	7000-55-3401	5.000
IC106 IC107 IC134 IC218 IC219	OP AMP,DUAL,LW NOISE PLAS,DIP-8,18Vdc 140KHz,9V/uS,SS#2	NE5532AN	SIG	7000-55-3201	5.000
IC108 IC109 IC419 IC420	QUAD POS NAND STATIC SENSITIVE	MC74HC00N	MOT	8000-74-0012	4.000
IC110 IC220 IC421	QUAD 2-INPUT EXCLUSV OR GATES STATIC SENSITIVE	SN74HC86	T-I	8000-74-8611	3.000
IC111	3-INPUT NAND GATE STATIC SENSITIVE	MC74HC10	MOT	8000-74-1001	1.000
IC112	OP.AMPL.,DUAL BIMOS, MINI DIP STATIC SENSITIVE	CA3240E	RCA	7000-32-4000	1.000
IC113	1 OF 8 DECODER/DEMUX STATIC SENSITIVE	MC74HC237N	MOT	8007-42-3710	1.000
IC114	STATIC SHIFT REG, 8 STATIC SENSITIVE	CD4021BE	RCA	8000-40-2110	1.000
IC115	8-INPUT OR/NOR GATE STATIC SENSITIVE	SN74HC4078A	T-I	8074-40-7800	1.000
IC116 IC221	VOLT REF,PREC,10V PLAS,DIP-8,1-100mV SS#2	REF-01CP	PMI	7000-00-0101	2.000
IC117 IC120 IC123 IC126	DAC,10-BIT STATIC SENSITIVE	DAC1020LCN	NAT	8000-10-2010	4.000

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
IC118 IC119 IC121 IC122 IC124 IC125 IC127 IC201 IC202 IC203 IC410 IC411 IC412 IC413 IC414	8-BIT SHIFT REGISTER STATIC SENSITIVE	MM74HC595N	NAT	8007-45-9510	15.000
IC129	FLOUR DISPLAY DRVR STATIC SENSITIVE	UDN-6118A	SPR	8000-61-1800	1.000
IC130 IC131	QUAD ANALOG SWITCH STATIC SENSITIVE	HI-201-5	HSD	8000-02-0100	2.000
IC132	DUAL JFET INPUT OPERATIONAL AMP STATIC SENSITIVE #2	LF412CN	NAT	7000-04-1210	1.000
IC133 IC140	DUAL OP AMP STATIC SENSITIVE #2	TL082CP	T-I	7000-00-8200	2.000
IC135 IC138	VOLT REG,FIXED,+15V PLAS,3 PIN(TO-220) 35Vdc,.1%,700mA,SS#2	UA78M15UC	FCD	7000-78-1500	2.000
IC136	VOLT REG,+5V STATIC SENSITIVE #2	MA78L05AWC	FCD	7000-78-0501	1.000
IC137	NEG VOLTAGE REG STATIC SENSITIVE #2	UA79M15AUC	FCD	7000-79-1500	1.000
IC139 IC222 IC424 IC425	POS. VOLT REG-3 TERM PLAS,TO-220AB,5 VOLT 500mA,7 W,5%,3-TERM	78M05U1C	FCD	7000-78-0500	4.000
IC142	HEX INVERTER STATIC SENSITIVE	SN74S04N	T-I	8000-74-0401	1.000
IC204 IC205 IC206 IC207 IC208	4-BIT BCD ADDER STATIC SENSITIVE	74F583	FCD	8007-45-8300	5.000
IC209 IC210 IC211 IC213	OCTAL D FLIP-FLOP STATIC SENSITIVE	MC74HC273N	MOT	8007-42-7300	4.000
IC214	DAC,8-BIT STATIC SENSITIVE	DAC-08EQ	AMD	8000-00-0800	1.000
IC223	VOLT REG, 15 STATIC SENSITIVE #2	MC78L15CP	MOT	7000-78-1510	1.000
IC224	VOLT,REG,FIXED,-15V PLAS,TO-226AA,-35Vdc 10%,Io=100mA,SS#2	MC79L15CP	MOT	7000-79-1510	1.000
IC401 IC415	PRESCALER,DIV,10/11 STATIC SENSITIVE	SP8680B	PLSSY	8000-86-8000	2.000
IC402	4-BIT BINARY COUNTER STATIC SENSITIVE	F10016DC	FCD	8001-00-1600	1.000
IC403 IC404	BCD DECADE CTR STATIC SENSITIVE	F10010DC	FCD	8001-00-1000	2.000
IC405 IC406	DECADE COUNTER STATIC SENSITIVE	MM74HC162	NAT	8007-41-6211	2.000
IC407 IC408	RES NTWK,DIP,TTL/ECL	4116R-008-001	BOU	4770-00-0021	2.000

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REV	ECN	BY	DA

POWER

S1001

LINE VOLTAGE SELECTOR	
SWITCH	CLOSED FOR
M	100/120 VAC
H	220/240 VAC
I	120 VAC
J	120/240 VAC
K	100/220 VAC

LINE FUSE R.P.

F1002
100/120 VAC
1.0 AT
220/240 VAC
5 AT

P1005 / J1005 — GRN, RED, BLK, WHT — 1 2 3 4 — BLU, BRO

J1006 — NEUTRAL, LINE, GRN/YEL CHASSIS GND — AC RECEPTACLE R.P. — W1001 — AC LINE PLUG

T1001 — WHT, BLK, VIO, BLU, BRO — CRT

P1001 / J1001 — 1 NC, 2, 3, 5, 6

F1001 1.0AT

CR1001

IC1001 REF-02 — +10V — R1003 39K — C1004 1MF

IC1002A TL082 — R1004 3.9K — C1005 1MF — R1008 13.0K — R1005 500 * ADJ — R1006 4.87K

Q1001 J232 — C1002 .005MF — R1002 1K — C1001 2700MF

Q1005 LM395 — C1003 100MF — CR1003

J1004 — 115VAC, BACKLIGHT ENA, GND, GND, GND

J1002 — 20VAC, +27V, +10V, +10V

R1022 120 1/2W — R1023 100 1/2W — R1028 2K — C1012 6.8MF — CR1004 12V — Q1007 2N3904 — C1013 10MF — E1001 BEC995 -8.0-12

R1021 3.3K — Q1006 2N3904 — R1029 47K — R1001 4.7K

R1024 10.0K — R1018 500 — R1011 10.0K — C1007 1MF — CR1005 — IC1002B TL082 — Q1003 2N3906 — -10V

R1012 9.7K — R1013 10K

R1015 1.2K — R1019 9.7K — C1006 .005MF — C1004 100MF — CR1005 — -10V

Q1004 LM395 — -10V

-27V, +8V, +8V, GND, GND

CR1008

CR1006, CR1007 — C1010 1000MF — 2700MF C1008

B1001 — RD, BK — P1003 / J1003

Q1005 MJE803 — R1025 820 — CR1010 12V — CR1011

IC1003 LM317 — R1016 150 — R1017 * — R1016 806 — R1015 * — C1011 10MF

* SELECT TO TRIM +8V OUTPUT, USE STABLE METAL FILM ONLY

NOTES:

1. CONNECTOR PIN NUMBERING DIAGRAMS

P1005 / J1005 — 1 2 3 4

PCB HEADERS (TYPICAL) — 1 2 3 4 5 ← LATCH

NOTE UNLESS OTHERWISE SPECIFIED

FIGURE 10-6

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN P FIELDER	DATE 07:06 1987	WAVETEK
MATERIAL	PROJENGR D CAMPBELL	APPVD	TITLE SCHEMATIC DPS-2F
FINISH WAVETEK PROCESS	RELEASE APPROV D CAMPBELL		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG	MODEL NO. 2500	DWG NO 0014-30-036
	SCALE M.85026.R0 /V10 FAB	CODE IDENT 34280	SIZE SHEET 6

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
2	CONN.,RECEPT.,3-PIN	6-86105-3	AMP	2112-25-0001	3.000
3	IC SKT,8-PIN,STKT LEG	2-640463-1	AMP	2112-00-0053	2.000
4	FUSE CLIP MF000-012	102071(TIN)	LIT	2410-05-1003	2.000
5	2500 POWER SUMPLY BD	1710-30-0061	W-I	1710-30-0061	1.000
6	GRIPLET-FUNNEL,.070 M1123-000	47299	BER	2112-19-0003	4.000
C1001 C1008	CAP,ELEC,35V,2700 UF	B0D272F035JA5	SPR	1510-27-7272	2.000
C1002 C1006	CAP,DISC,100V,.005UF TAPE AND REEL	TG-D50	SPR	1510-10-2502	2.000
C1003 C1009	CAP,ELEC,25V,100UF TAPE AND REEL	RE100MF25V20%	ELNA	1510-23-4101	2.000
C1004 C1005 C1007	CAP,TANT,25V,1UF	100ME105K25A2	ACI	1510-21-7010	3.000
C1010	CAP,ELEC,16V,10000UF	ECE51CV103S	PNSNC	1510-27-3103	1.000
C1011	CAP,TANT,25V,10UF	100ME106M20C2	ACI	1510-21-7100	1.000
C1012	CAP,TANT,25V,68UF	T353L686K025AS	UNCAR	1510-22-7680	1.000
C1013	CAP,TANT,25V,10UF	T368B106K025AS	UNCAR	1510-24-4100	1.000
CR1001	DIODE,RECT BRDG,GP 312-02,V=100V,IO=2A SUR I=60A,SS#2	MDA201	MOT	4806-02-0017	1.000
CR1002 CR1004	DIODE,SIGNAL,GP AXIAL,V=75V,IO=10mA CT=4pF,SS#2	1N914	G-E	4807-01-0914	2.000
CR1003 CR1005 CR1008 CR1011	DIODE,RECT,GP DO-15,V=400V,IO=1.0A SUR I=30A,SS#2	1N4004	P-C	4808-01-4004	4.000
CR1006 CR1007	DIODE,RECT,GP AXIAL,V=200,IO=5.0A SUR I=225A,SS#2	1N5624	G-E	4808-01-5624	2.000
CR1009 CR1010	DIODE,ZENER,1W,GP DO-41,V=12,IT=21mA IF=76mA,+/-5%,SS#2	1N4742A	MOT	4801-02-0003	2.000
E1001	PWR SUPPLY,13.8 VDC FOR BACK LIGHT PKG 7-9 SQ IN MAX	945-8.0-12	BALL	3010-90-0055	1.000
IC1001	15 VOLTAGE REFERENCE	REF02CP	PMI	7000-00-0203	1.000
IC1002	DUAL OP AMP STATIC SENSITIVE #2	TL082CP	T-I	7000-00-8200	1.000
Q1001	JFET-N,TO-92,AUD AMP VGS=40,IDSS=10mA P=350mW,SS#1	E232	SCX	4902-00-2320	1.000

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
Q1003	PNP,TO-92,GP AMP/SW F=300,V=40,Icex=50nA P=625mW,hFE=100,SS#2	2N3906	T-I	4901-03-9060	1.000
Q1005	NPN,TO-126,DRLNG PWR F=1M,V=80,Iceo=100uA P=40W,hFE=750, SS#2	MJE803	MOT	4902-00-8030	1.000
Q1006 Q1007	NPN,TO-92,GP AMP/SW F=300,V=40,Icex=50nA P=625mW,hFE=100,SS#2	2N3904	NAT	4901-03-9040	2.000
R1001 R1012 R1014	RES,C,1/4W,5%,4.7K	CF1/4-4.7K	ASE	4700-15-4701	3.000
R1002	RES,C,1/4W,5%,1K	CF1/4-1K	ASE	4700-15-1001	1.000
R1003	RES,C,1/4W,5%,39K	CF1/4-39K	ASE	4700-15-3902	1.000
R1004	RES,MF,1/8W,1%,4.87K	RN55D-4.87K	MILSP	4701-03-4871	1.000
R1005	TRM,CM,L,500,10%,PC 11,PN,CW,.375H,.200W .375L,SA	3386S-1-501	BOU	4610-00-1501	1.000
R1006	RES,C,1/4W,5%,3.9K	CF1/43.9K	ASE	4700-15-3901	1.000
R1008	RES,MF,1/8W,1%,13.0K	RN55D-13.0K	MILSP	4701-03-1302	1.000
R1009 R1011	RES,MF,1/8W,1%,10K	RN55D-10K	MILSP	4701-03-1002	2.000
R1010	TRM,CM,L,200,10%,PC 1T,PN,CW,.375H,.200W .375L,SA	3386S-1-201	BOU	4610-00-1201	1.000
R1013	RES,C,1/4W,5%,10K	CF1/4-10K	ASE	4700-15-1002	1.000
R1015	RES,C,1/4W,5%,1.2K	CF1/4-1.2K	ASE	4700-15-1201	1.000
R1016	RES,MF,1/8W,1%,150 TAPE AND REEL	RN55D-150	MILSP	4701-03-1500	1.000
R1018	RES,MF,1/8,1%,806	RN55D-806	MILSP	4701-03-8060	1.000
R1020	RES,C,1/4W,5%,24K	CF1/4-24K	ASE	4700-15-2402	1.000
R1021	RES,C,1/4W,5%,3.3K	CF1/4-3.3K	ASE	4700-15-3301	1.000
R1022	RES,C,1/2W,10%,120	EB1215	A-B	4700-25-1200	1.000
R1023	RES,C,1/2W,5%,100	CF1/2-100	ASE	4700-25-1000	1.000
R1024	RES,C,1/4W,5%,47K	CF1/4-47K	ASE	4700-15-4702	1.000
R1025	RES,C,1/4W,5%,820	CF1/4-820	ASE	4700-15-8200	1.000
SCH	SCH,POWER SUPPLY, DFS-2F	0014-30-0365	W-I	0014-30-0365	1.000

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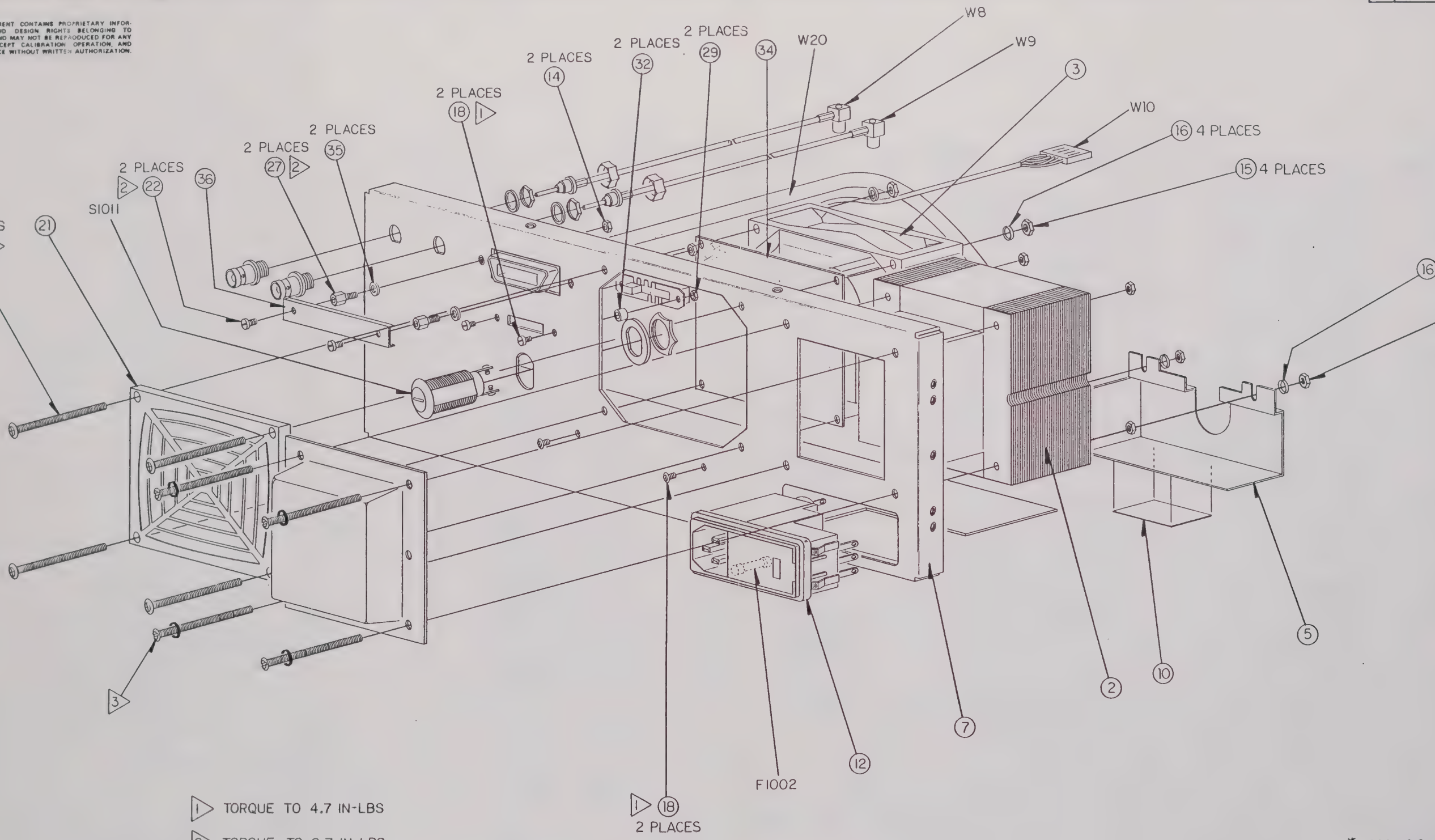
REV	ECN	BY	D



1 TORQUE TO 4.7 IN-LBS

2 TORQUE TO 8.7 IN-LBS

3 TORQUE TO 17.8 IN-LBS

REFERENCE BOM #1115-00-0045

FIGURE 10-6A1

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B Naylon	DATE 2/86	WAVETEK
MATERIAL	PROJ ENGR		TITLE DPS2F POWER SUPPLY — DRAWING —
FINISH WAVETEK PROCESS	RELEASED APPROV	11/86	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG		MODEL NO 2500 DWG NO 0012-30-00
	SCALE FULL	CODE IDENT 34280	SHEET 1

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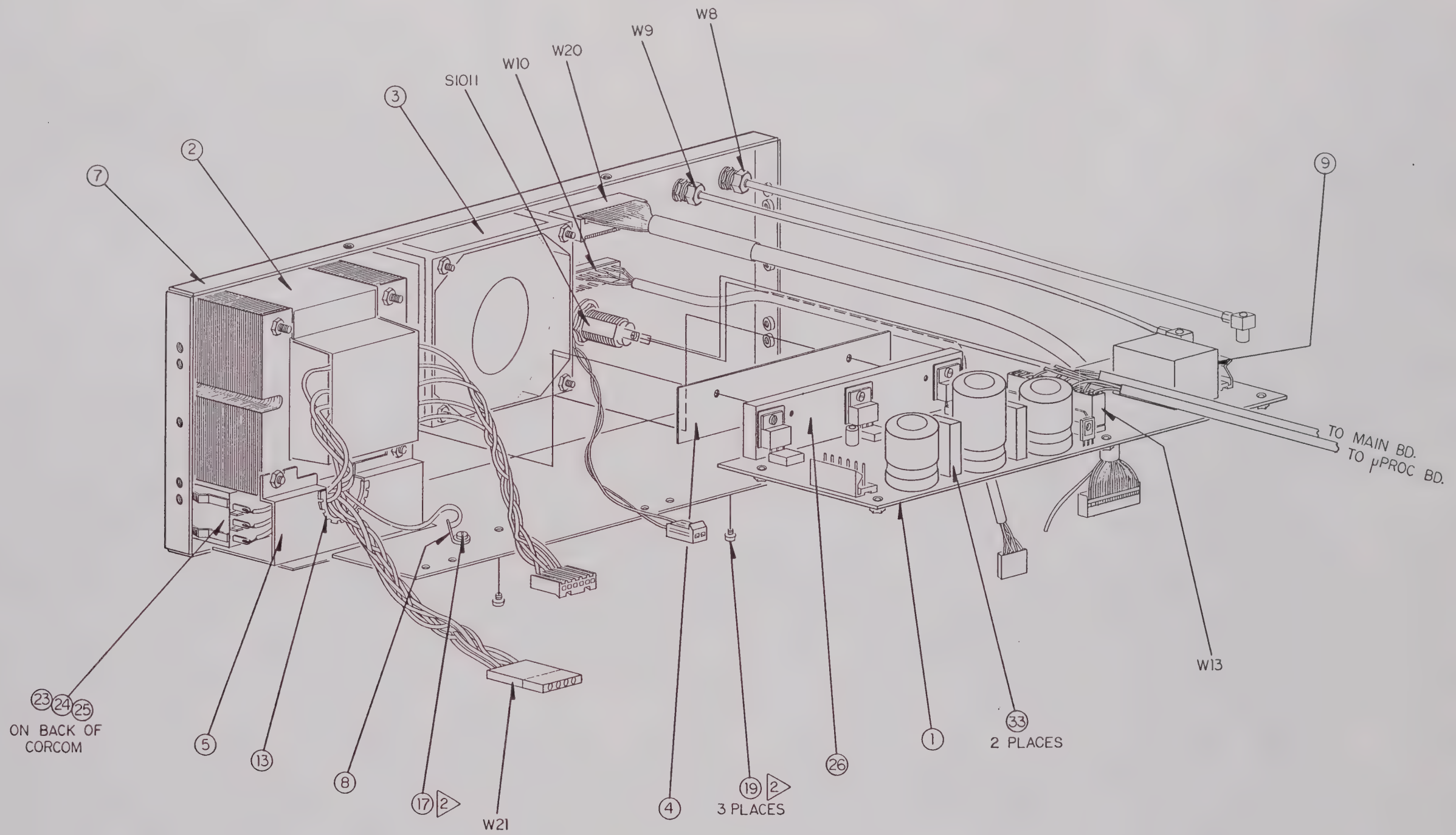
REV	ECN	BY	DATE	APP



REFERENCE BOM *1115-00-0045

FIGURE 10-6A2

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE 2/86	WAVETEK				
MATERIAL	PROJ ENGR		TITLE	DPS2F POWER SUPPLY — DRAWING —			
	RELEASE APPROV						
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX						
	DO NOT SCALE DWG		MODEL NO 2500	DWG NO. 0012-30-0027	REV		
	SCALE FULL		CODE IDENT 34280	SHEET 2 OF 2			

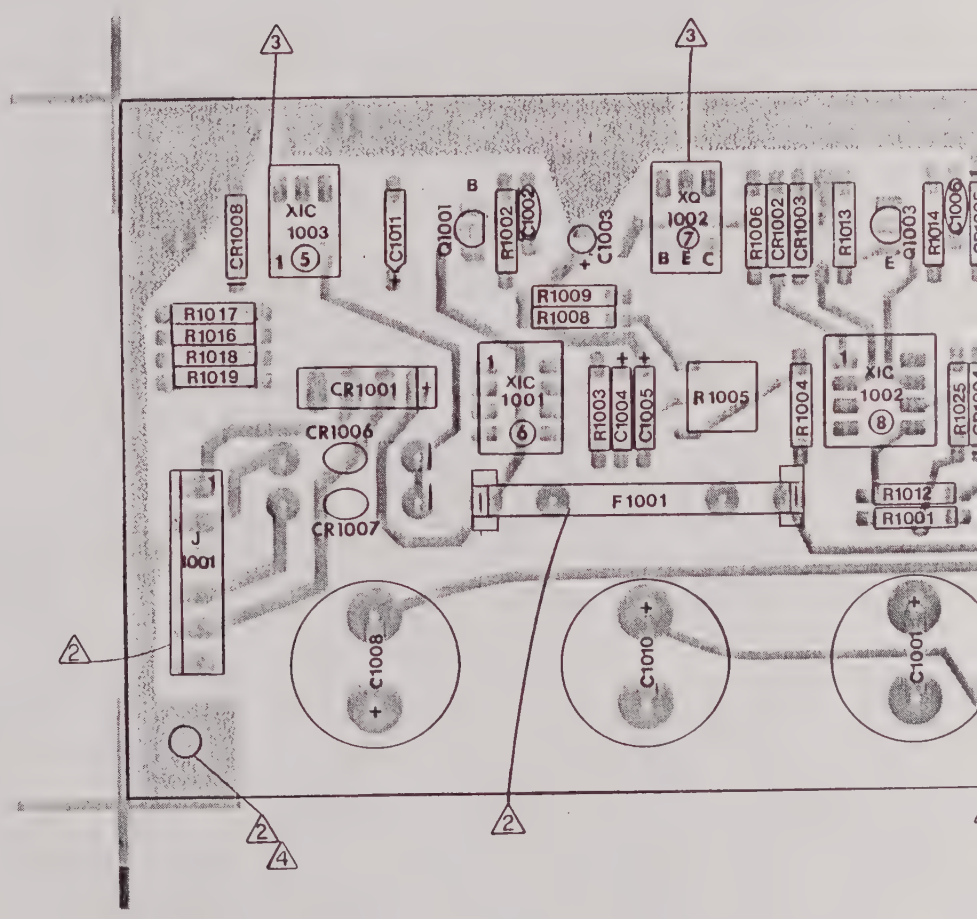
8	7	6	5	4	3	2	1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
1	PC ASSY,DPS2F,2500	DPS2F-PC-2500	W-I	1118-00-0171	1.000
2	XFMR ASSY,DPS2D	DPS2D-XFMR	W-I	1219-00-0480	1.000
3	DPS2F FAN ASSYPER B/P	DPS2F-FAN	W-I	1219-00-0583	1.000
4	INSULATORPER B/P	1410-01-4760	W-I	1410-01-4760	1.000
6	LINE SHIELDPER B/P	1410-30-8290	W-I	1410-30-8290	1.000
7	REAR PANEL,2500 PER B/P	1410-80-1930	W-I	1410-80-1930	1.000
8	GROUND LUG,#6,INT NG102-600	38-111	F-S	2112-03-0003	1.000
9	CAUTION DECAL	2410-04-0707	W-I	2410-04-0707	1.000
10	WARNING DECAL	2410-04-0708	W-I	2410-04-0708	1.000
11	CABLE TIE,4	PLTIM-MP	PAND	2810-00-0010	2.000
12	FUSEHOLDER/PWR ENTRY MODULE	PE712003	CRTIS	2410-05-0045	1.000
13	CAT GROMMET, 2.5 IN FROM:2810-10-0021	2810-10-0047	W-I	2810-10-0047	1.000
15	NUT,8-32,STD	8009NP	F-S	2810-14-8101	6.000
16	#,INT,LOWASHER HW101-800	13052P	F-S	2810-24-8000	6.000
17	SCW,PFH,6-32X1/8	19040NP	F-S	2810-55-6102	1.000
18	SEMS-PFH-INT 4-40 X 3/8 NPPER B/P	PER DESC2810-57-4106	F-S	2810-57-4106	4.000
19	SEMS-PFH-INT 6-32 X 1/4 NPPER B/P	PER DESC2810-57-6104	F-S	2810-57-6104	3.000
20	SCW,PFH,8-32X1-3/4BK	19074-BK OXIDE	F-S	2810-65-8128	4.000
21	FAN GUARD	FF-325G	AFP	3010-13-0017	1.000
22	SCREW,PH,M3.5X.6X6MM	PER DESC2810-23-0122	S-S	2810-23-0122	2.000
23	WIRE,BUSS,18 GA.	8019	BEL	6010-91-8000	1.750
24	SLEEVING,TEF,TW,18GA 100FT PER SPL.	TT250-18	CLFX	6011-21-6000	1.500
25	WIRE,18,UL1015,GN/YL.	UL1015-18-GN/YL	ULSP	6013-11-8545	7.000
26	HEATSINK ASSY,DPS2F	DPS2F-HEATSINK	W-I	1218-00-0274	1.000
28	SEMS-PFH-INT 4-40 X 3/16 NPPER B/P	PER DESC2810-57-4103	F-S	2810-57-4103	2.000
29	NUT,4-40,HN101-400	8002A-NP	F-S	2810-14-4100	2.000
30	SPACER,ROUND,4X1/8 X3/160D,HD103-402	10810ONP	F-S	2810-04-4002	2.000

WAVETEK PARTS LIST	POWER SUPPLY,DPS2F, 2500	1115-00-0045 PAGE: 1	G REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
31	SEMS-PFH-INT 4-40 X 1/4 NPPER B/P	PER DESC2810-57-4104	F-S	2810-57-4104	2.000
32	SPACER	S2B4-N01-F05A-E	UNIC	2810-04-4009	2.000
33	FOAM FOR CAPS FROM:3210 99-0017	1410-01-4990	W-I	1410 01-4990	2.000
34	FAN SCREEN FROM:3210-02-0571 PER B/P	1410-30-8240	W-I	1410-30-8240	1.000
35	INT,LOWASHER,6 HW101-600	1304ZP	F-S	2810-24-6000	2.000
36	GP1B CONN COVER PER B/P	1410-01-4980	W-I	1410-01-4980	1.000
F1002	FUSE,SLO BLO,1 AMP, 250V	MDL-1	BUS	2410-05-0005	1.000
S1011	KEY SWITCH,SPST	SWK-13-2 AL101	ALC	5106-00-0045	1.000
W08	CABLE ASSY, 20 IN	WX2500-W8	W-I	1217-80-0117	1.000
W09	CABLE ASSY, 21 IN	WX2500-W9	W-I	1217-80 0118	1.000
W10	RF MHZ SWITCH CABLE, 2500	WY2500-W10	W-I	1219-00-0599	1.000
W13	DC POWER CABLE,2500	WY2500-W13	W-I	1219-00-0601	1.000
W20	CABLE ASSY,GP1B PER B/P	WX2500-W20	W-I	6011-60 0075	1.000
W21	CORCOM HARNESS,2202	2202-CORCOM HARNESS	W-I	1219-00 0592	1.000
W1001	LINE CORD,3-COND,SVT 18 GA,7-1/2 FT,W/REC EUROPEAN COLOR CODE	6011-80-0006	ECMC	6011-80-0006	1.000

WAVETEK PARTS LIST	POWER SUPPLY,DPS2F, 2500	1115-00-0045 PAGE: 2	G REV



1. METAL THIS SIDE
2. DO NOT WAVE SOLDER
3. BEVELED ENTRY THIS SIDE 3 PLACES
4. SWAGE NUTS 4 PLACES

NEXT ASSY	USED
APPLICATION	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		REV. 00	8-86	CK

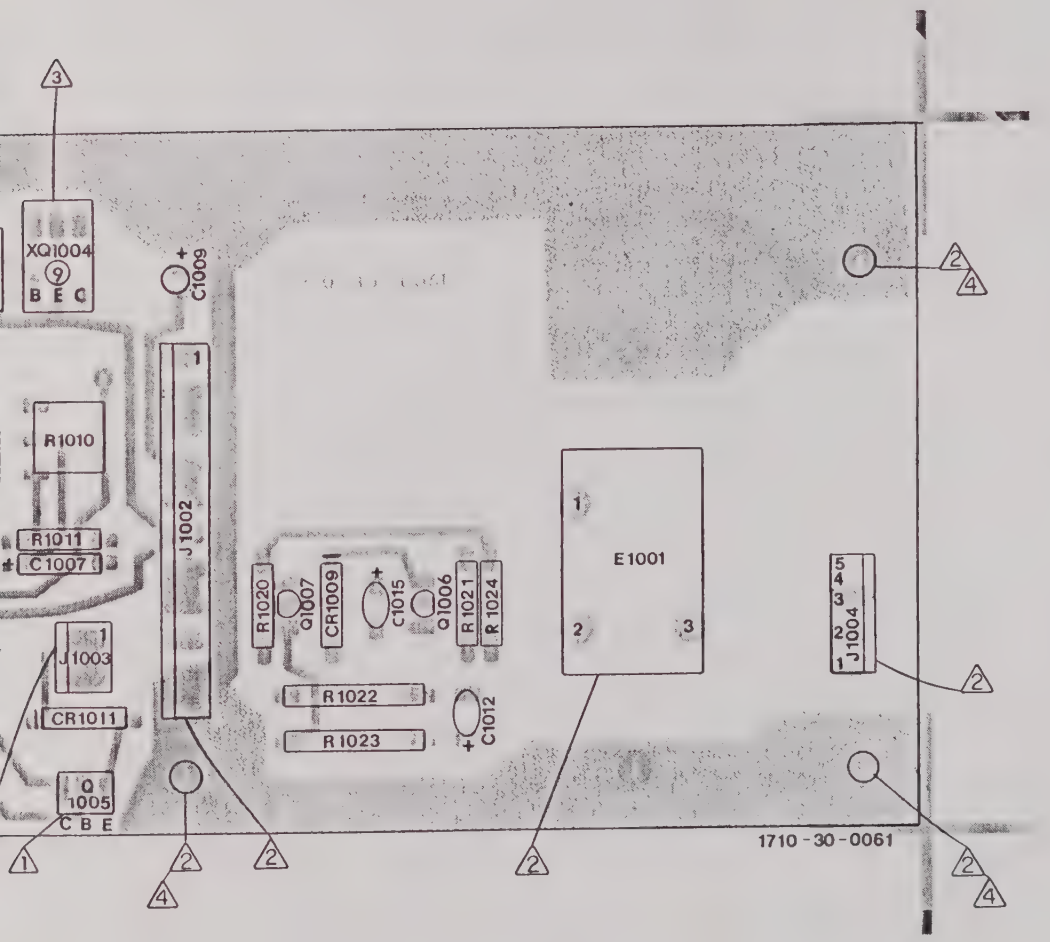


FIGURE 10-6B

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN C. KEISER	10-85
CHECKED	

10-18

WAVETEK INDIANA, INC.

2500 POWER SUPPLY
PART LAYOUT

SIZE	CODE IDENT NO	DRAWING NO.
C	34280	0012-20-0031

SCALE | SHEET / OF /

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
2	PC BOARD ASSY,2500	2500-PC	W-I	1218-00-2510	1.000
3	STANDOFF,SWAGE,.188, NO. 6	350-3928-10-07-00	CAM	2810-05-0015	4.000
F1001	FUSE,SLO BLO,1 AMP, 250V	MDL-1	BUS	2410-05-0005	1.000
J1001	PLUG,6-PIN KONEKTON MC000-075	09-65-1061	MOL	2112-05-0002	1.000
J1002	11 PIN LOCKING PLUG MC000-137	09-65-1111	MOL	2112-05-0005	1.000
J1003	CONN.,MALE,2-PIN	09-65-1021	MOL	2112-05-0010	1.000
J1004	CONN.,MALE 5-PIN MC000-070	09-65-1051	MOL	2112-05-0006	1.000

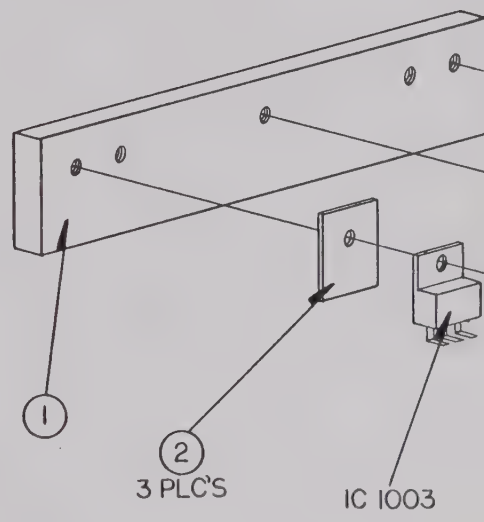
WAVETEK PARTS LIST	PC ASSY,DFS2F,2500	1118-00-0171 PAGE: 1	A REV

D

C

B

A



1 TORQUE TO 4.7 IN-LBS

1216-00-0274	
NEXT ASSY	
APPLIC	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

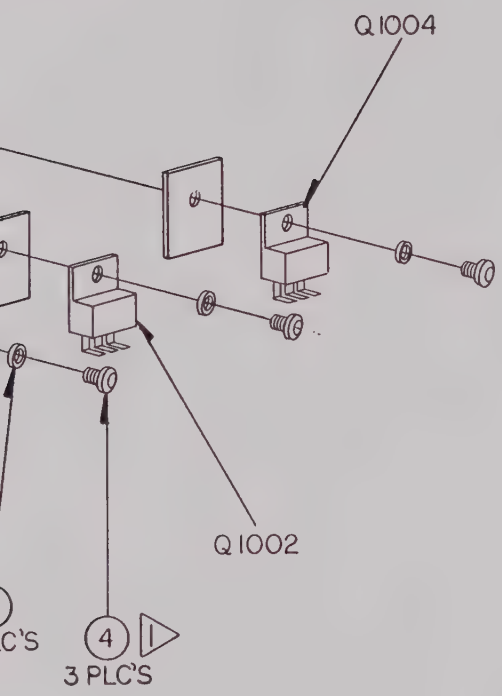


FIGURE 10-6C

	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN	7/86
CHECKED	8/86
	8/1/86

10-20

WAVETEK INDIANA, INC.

HEATSINK ASSY. DRAWING

SIZE	CODE IDENT NO.	DRAWING NO.
C	34280	0012-20-0039

SCALE N/A | SHEET | OF |

REFERENCE DESIGNATORS	PART DESCRIPTION >	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
1	POWER SUPPLY HEATSNK 2500PER B/P	1410-01-4750	W-I	1410-01-4750	1.000
2	MICA INSULATOR	B00853A001	MOT	2810-11-0004	3.000
3	SHLDR WSHR, TO-220	B51547F015	MOT	2810-11-0031	3.000
4	SCW,PPH,4-40X1/4	19022NP	F-S	2810-55-4104	3.000
IC1003	ADJ REG,1.2V-37V PLAS,TO-220,1.5A=Io 15W,0.1Z,SS#2	LM317T	NAT	7000-03-1700	1.000
Q1002 Q1004	PROT PWR DARLINGTON STATIC SENSITIVE #2	LM395T	NAT	4902-00-3950	2.000

WAVETEK PARTS LIST	HEATSINK ASSY,DPS2F	1216-00-0274 PAGE: 1	2 REV

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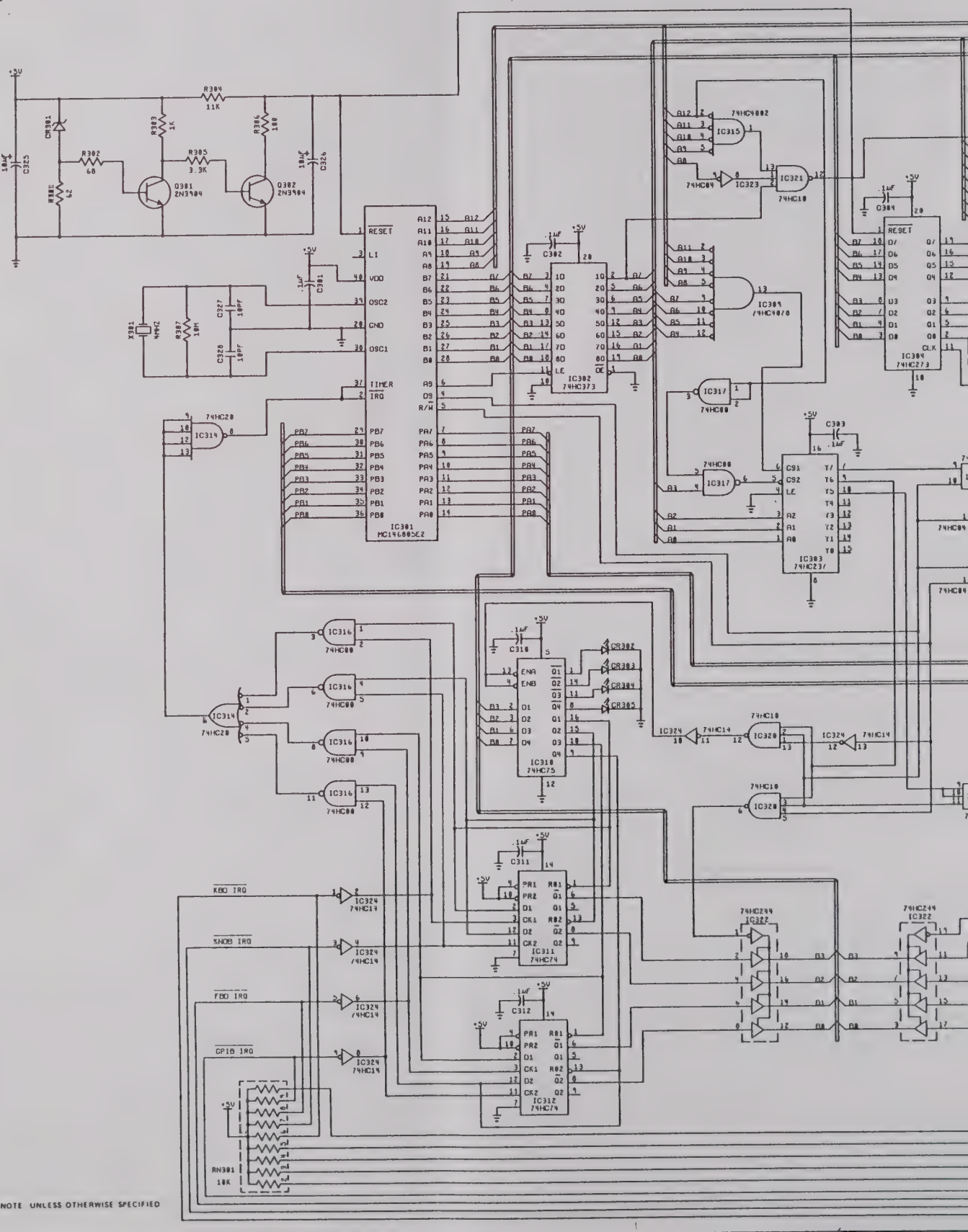

NOTE UNLESS OTHERWISE SPECIFIED

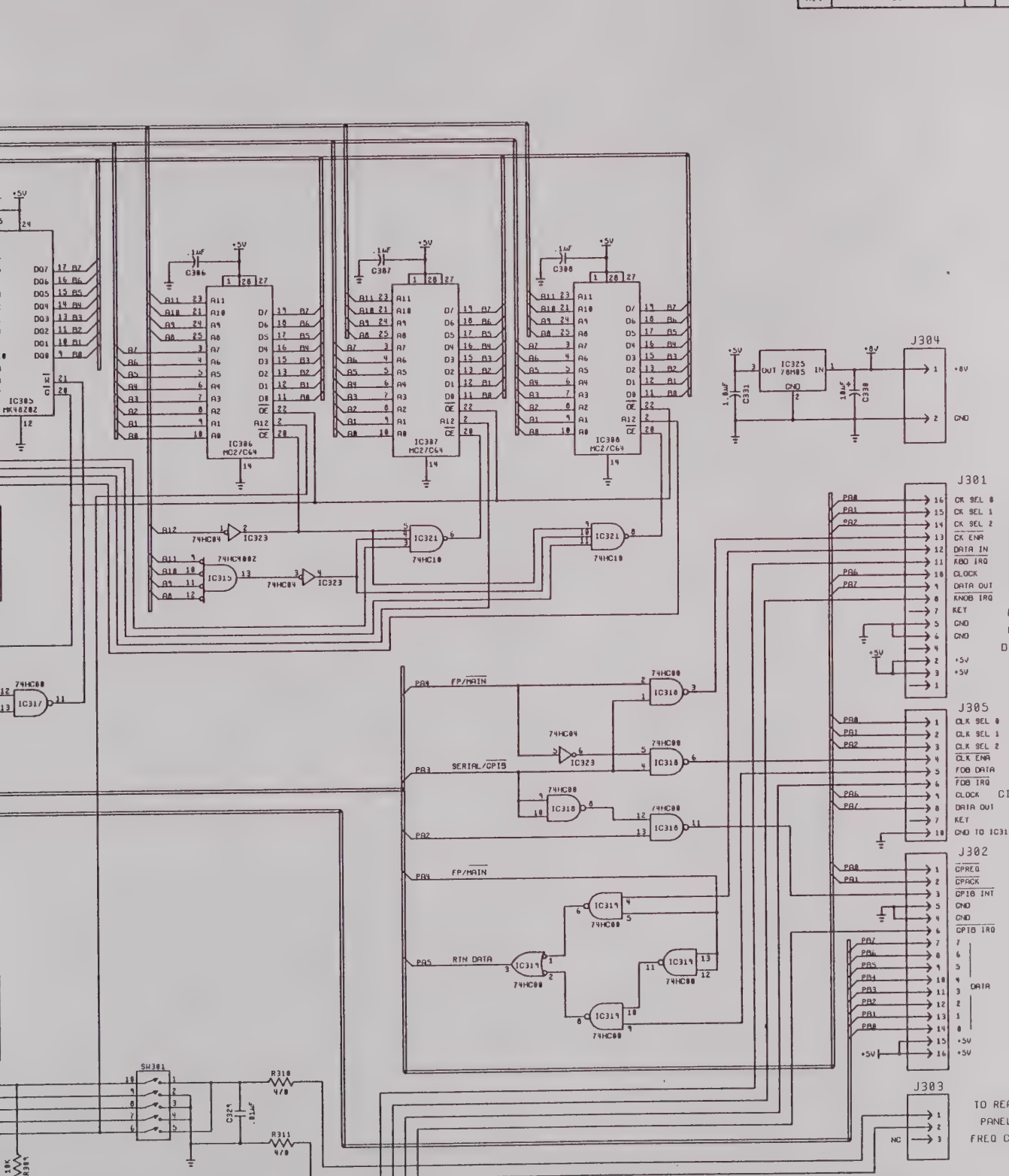

FIGURE 10-7

NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL UNMARKED CAPS ARE .1μF.
2. BYPASS CAPS ARE .1μF.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B ABEL	DATE 09:3	WAVETEK
MATERIAL	PROJ ENGR T DUDZIAK	6 JA 198	TITLE MFG / ENGR CHECK SET
	RELEASE APPROV T DUDZIAK		SCHEMATIC
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ANGLES XX		μPROCESSOR BO
	DO NOT SCALE DWG	MODEL NO 2500	DWG NO. 0014-30-03
	SCALE N/H	CODE IDENT 34280	C11A SHEET 6
	TM.05020.R00 /V53.FAB		

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
C301 C302 C303 C304 C305 C306 C307 C308 C309 C310 C311 C312 C313 C314 C315 C316 C317 C318 C319 C320 C321 C322 C323	.1 MF 20%,50V,GENERL PURPOSE AXIAL LEAD TAPE AND REEL	SA205E1042AA	AVX	1510-17-1104	23.000
C325 C326 C330	CAP,TANT,25V,10UF	100DE106M20C2	ACI	1510-21-7100	3.000
C327 C328	10 PF,100V,NPO AXIAL LEAD TAPE AND REEL	C410C100J1G5CA	KEMET	1510-17-1100	2.000
C329	.01 MF 10%,50V STABL AXIAL LEAD CAP TAPE AND REEL	C410C103K5R5CA	KEMET	1510-17-1103	1.000
C331	CAP,TANT,25V,1UF	100DE105K25A2	ACI	1510-21-7010	1.000
CR301	DIODE,ZENER,0.5W AXIAL,V=3.6V +/-5%,SS#2	1N5227	T-I	4801-01-5227	1.000
CR302 CR303 CR304 CR305	(D)LED,RED,T-1,5V RESISTOR,INTEGRATED	HNLP-1600	H-P	4B10-02-0017	4.000
GND01	HEADER,1-PIN,STRT REF:2112-07-0000	65501-401	BER	2112-07-0020	1.000
IC301	8-BIT MICROPROCESSOR CMOSSTATIC SENSITIVE	MC146805E2	MOT	8014-68-0310	1.000
IC302	OCTAL 3-STATE LATCH STATIC SENSITIVE	MC74HC373N	MOT	8007-43-7311	1.000
IC303	1 OF 8 DECODER/DEMUX STATIC SENSITIVE	MC74HC237N	MOT	8007-42-3710	1.000
IC304	OCTAL D FLIP-FLOP STATIC SENSITIVE	MC74HC273N	MOT	8007-42-7300	1.000
IC305	ZEROPOWER RAM 2K X 8 CMOSSTATIC SENSITIVE	MK48Z02B-20	MOSTK	8000-48-0210	1.000
IC309	8-INPUT OR/NOR GATE STATIC SENSITIVE	SN74HC4078A	T-I	8074-40-7800	1.000
IC310	4-BIT BISTABLE LATCH STATIC SENSITIVE	MC74HC75	MOT	8000-74-7500	1.000
IC311 IC312	2-D TYP,POS EDG TRIG FLIP-FLOP W/CLR&PRE-SET,STATIC SENSITIVE	MC74HC74	MOT	8000-74-7403	2.000
IC314	DUAL 3-INPUT POSITIVE NAND GATE STATIC SENSITIVE	MC74HC20	MOT	8000-74-2000	1.000
IC315	DUAL 4-INPUT POS-NOR GATESSTATIC SENSITIVE	SN74HC4002N	T-I	8074-40-0210	1.000
IC316 IC317 IC318 IC319	QUAD POS NAND STATIC SENSITIVE	MC74HC00N	MOT	8000-74-0012	4.000

REFERENCE DESIGNATORS	PART DESCRIPTION	ORI
IC320 IC321	3-INPUT NAND GATE STATIC SENSITIVE	MC7
IC322	OCTAL BUF/LN DRVR STATIC SENSITIVE	MC7
IC323	HEX INVERTER, STATIC SENSITIVE	MC7
IC324	HEX SCHMITT-TRIGGER INVERTERS STATIC SENSITIVE	SN7
IC325	POS. VOLT REG-3 TERM PLAS,FO-220AB,5 VOLT 500mA,7 W,5%,3-TERM	78M
J301	16 PIN STRIP RECEPT	CAS
J302	HDR,DBL,STRT,GOLD,16	65
J303	HEADER,3-PIN STRT REF:2112-07-0000	65
J304	CONN.,MALE,2-PIN	09-
J305	HDR,DBL,STRT,GOLD,10	65
KIT	EPROM KIT,UPROC,2500	12
Q301 Q302	NPN,TO-92,GP AMP/SW F=300,V-40,Icex=50nA P=625mW,hFE=100,SS#2	2N
R301	RES,C,1/4W,5%,62	CF1
R302	RES,C,1/4W,5%,68	CF1
R303	RES,C,1/4W,5%,1K	CF1
R304	RES,C,1/4W,5%,11K	RCF
R305	RES,C,1/4W,5%,3.3K	CF1
R306	RES,C,1/4W,5%,100	CF1
R307	RES,C,1/4W,5%,10M	CB1
R309	RES,C,1/4W,5%,10K	CF1
R310 R311	RES,C,1/4W,5%,470	CF1
RN301	RES,NW,10K,SIP,2% 1-1/4W,BUSSED,9 RES TC=100PPM	750
SCH	SCH,UPROC BD,2500	001
SW301	SWITCH DIP 5 SPST	76B
X301	CRYSTAL, 4 MHZ	MPD

MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
C10	MOT	8000-74-1001	2.000
C244N	MOT	8007-42-4411	1.000
C04N	MOT	8000-74-0411	1.000
C14N	T-I	8000-74-1411	1.000
U1C	FCD	7000-78-0500	1.000
-SLP-TSD	C-A	2112-13-0016	1.000
-116	BER	2112-07-0079	1.000
-403	BER	2112-07-0001	1.000
-1021	MDL	2112-05-0010	1.000
-110	BER	2112-07-0078	1.000
00-0616	W-I	1219-00-0616	1.000
4	MAT	4901-03-9040	2.000
-62	ASE	4700-15-6209	1.000
-68	ASE	4700-15-6809	1.000
-1K	ASE	4700-15-1001	1.000
1K-0B	CII	4700-15-1102	1.000
-3.3K	ASE	4700-15-3301	1.000
-100	ASE	4700-15-1000	1.000
5	A-B	4700-15-1005	1.000
-10K	ASE	4700-15-1002	1.000
-470	ASE	4700-15-4700	2.000
01-R10K	CTSBR	4770-00-0012	1.000
-30-0349	W-I	0014-30-0349	1.000
5	G-H	5112-00-0002	1.000
)	CTS-E	2310-00-0451	1.000

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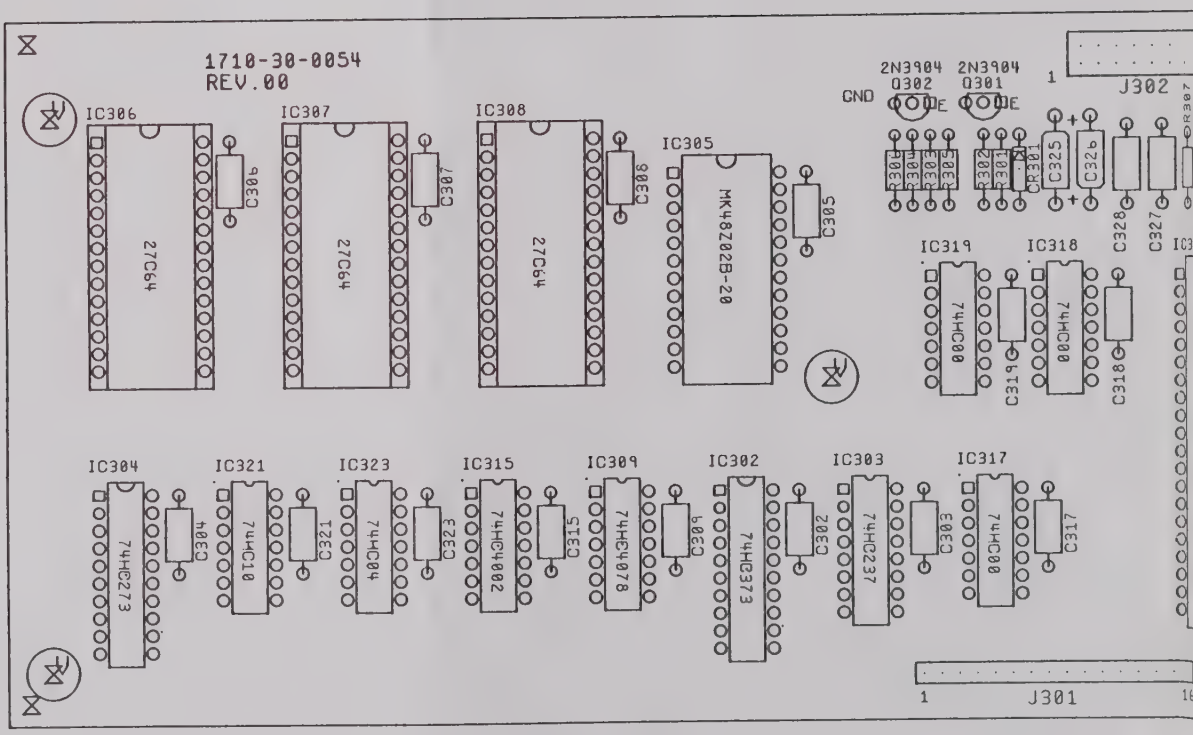

NOTE UNLESS OTHERWISE SPECIFIED

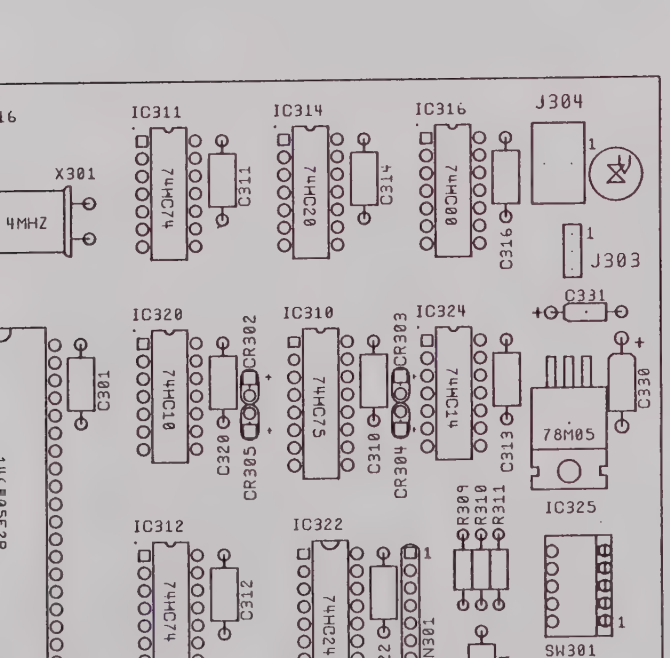

FIGURE 10-7A

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B ABEL	DATE 09:2
MATERIAL	PROJ ENGR T STUCKER	6 JAN 198
	RELEASE APPROV T DUDZIAK	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX	
	DO NOT SCALE DWG	
	SCALE 2:1	
	TM.85020.R00 /V53.FAB	

WAVETEK

TITLE MFG / ENGR CHECK SET

TOP ASSEMBLY D
µPROCESSOR BOA

MODEL NO.	DWG NO.
2500	0012-30-00
CODE IDENT 34280	C2A SHEET 3

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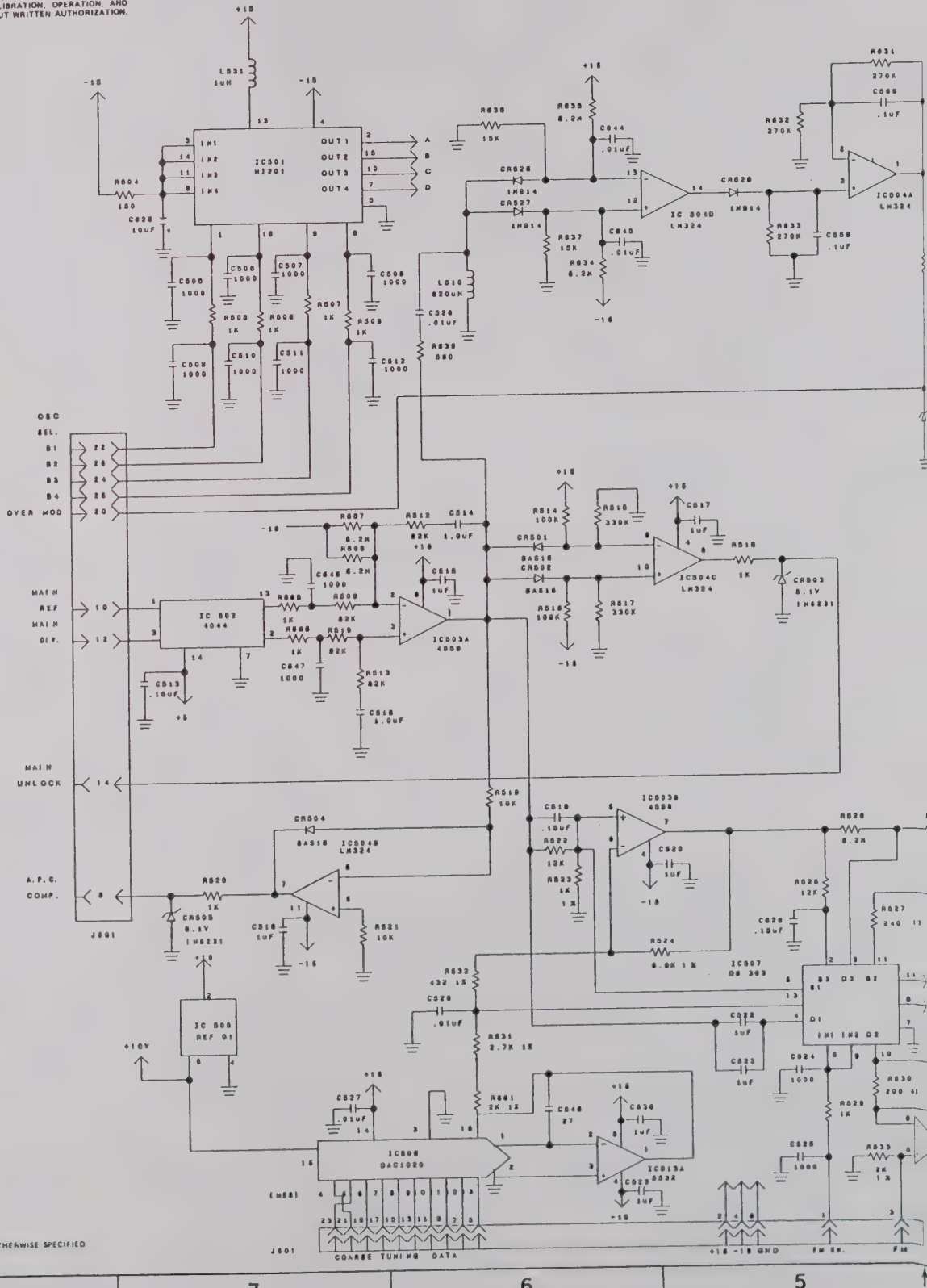

NOTE UNLESS OTHERWISE SPECIFIED

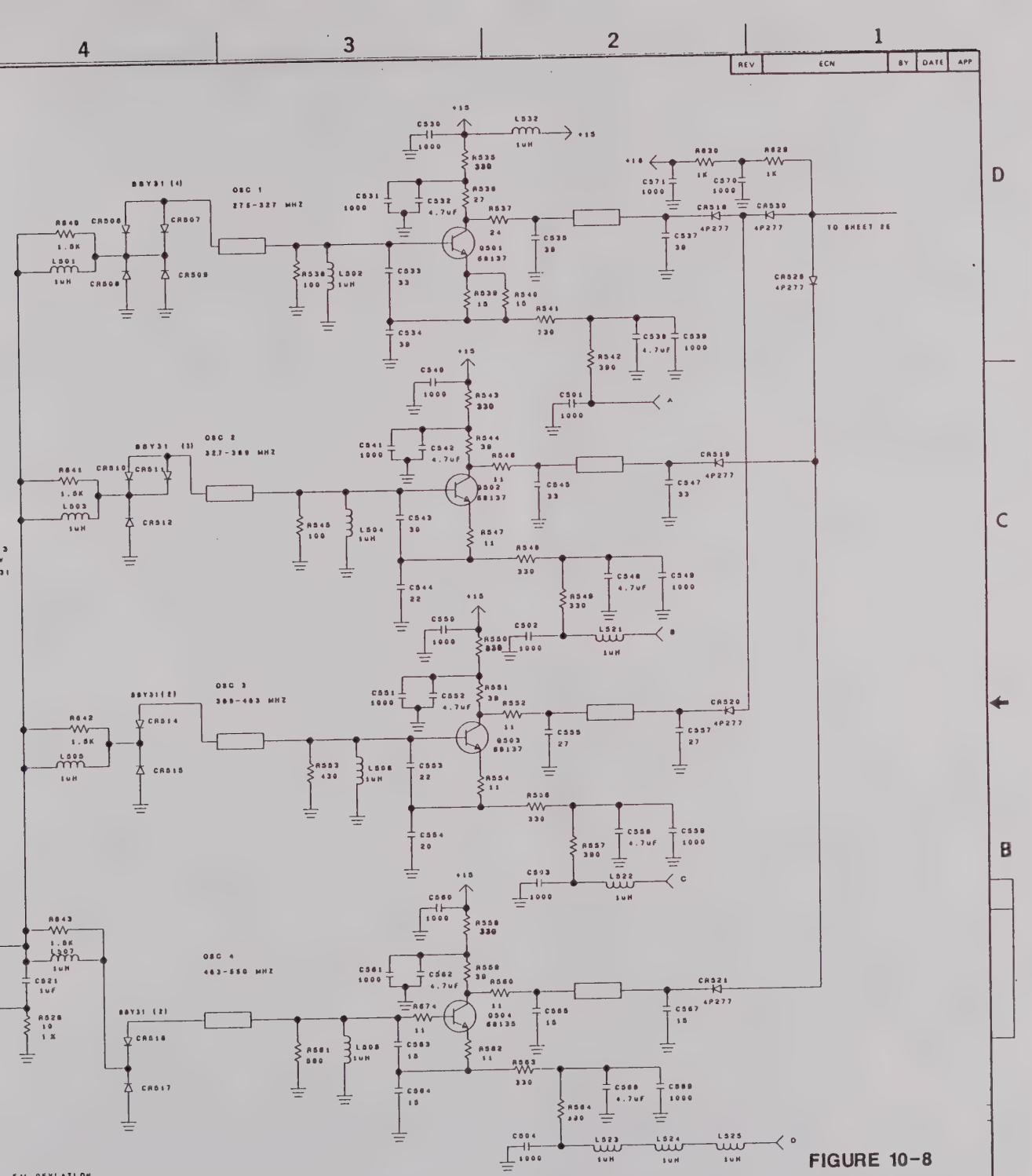

FIGURE 10-8

REV	ECN	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN C. KEISER	DATE 6-87	WAVETEK
MATERIAL	PROJ ENGR		TITLE OSCILLATOR BD. MAIN LOCK AND VCO SECTION
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG		MODEL NO 2500 / DWG NO 0014-30-0355 / REV E
	SCALE		CODE IDENT 34280 / SHEET 1 OF 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
C514 C515 C516 C517 C518 C520 C521 C522 C523 C529 C536 C617 C618 C619 C628	CAP,MON,50V,1UF	3420-050-E105M	AER	1510-11-3105	15.000
C532 C538 C542 C548 C552 C558 C562 C568	CAP,MON,50V,4.7UF	SR505E475MAA	AER	1510-11-3475	8.000
C621 C622 C623 C624 C625	CAP,TANT,25V,10UF	100ME106M20C2	ACI	1510-21-7100	5.000
C626	CAP,TANT,25V,10UF	T368B106M025AS	UNCAR	1510-24-4100	1.000
CR503 CR505 CR513 CR525	DIODE,ZENER,500mW,GP DO-35,V=5.1,IT=20mA IF=89mA,+/-20Z,SS#2	1N5231	MOT	4801-01-5231	4.000
CR526 CR527 CR528	DIODE,SIGNAL,GP AXIAL,V=75V,IO=10mA CT=4pF,SS#2	1N914	G-E	4807-01-0914	3.000
IC501	QUAD ANALOG SWITCH STATIC SENSITIVE	HI-201-5	HSD	8000-02-0100	1.000
IC502 IC509	PHASE DET,FCD ONLY STATIC SENSITIVE	11C44DC ONLY	FCD	8000-11-4400	2.000
IC503 IC508	DUAL OP AMP,RAY ONLY STATIC SENSITIVE #2	RC4558NB-RAY	RAY	7000-45-5801	2.000
IC504	OP AMP,QUAD,LOW PWR PLAS,DIP-14,30V 1MHz,45mAdc,SS#2	LM324N	NAT	7000-03-2400	1.000
IC505	VOLT REF,PREC,10V PLAS,DIP-8,+-100mV SS#2	REF-01CP	PMI	7000-00-0101	1.000
IC506	DAC,10-BIT STATIC SENSITIVE	DAC1020LCN	NAT	8000-10-2010	1.000
IC507	ANALOG SWITCH STATIC SENSITIVE	DG303ACJ	SCX	8000-03-0310	1.000
IC510	VOLT,REG,FIXED,-15V PLAS,TO-226AA,-35Vdc 10Z,Io=100mA,SS#2	MC79L15CP	MOT	7000-79-1510	1.000
IC511	VOLT REG,+5V STATIC SENSITIVE #2	MA78L05AWC	FCD	7000-78-0501	1.000
IC512	VOLT REG, +15 STATIC SENSITIVE #2	MC78L15CP	MOT	7000-78-1510	1.000
IC513	OP AMP,DUAL,LW NOISE PLAS,DIP-8,18Vdc 140KHz,9V/uS,SS#2	NE5532AN	SIG	7000-55-3201	1.000
IC514	DUAL JFET INPUT OPERATIONAL AMP STATIC SENSITIVE #2	LF412CN	NAT	7000-04-1210	1.000
J501A J501B	MOD,RECEPT,PC MT,.1 CTR,14 PIN,TOP ENTRY FROM:2112-35-0011	2112-35-0013	W-I	2112-35-0013	2.000

REFERENCE DESIGNATORS	PART DESCRIPTION
KIT	HYBRID PT KT,OSC BD, 2500
L501 L503 L505 L507 L513 L521 L522 L523 L524 L525 L526 L528 L531 L532	CHOKE,COATED,1UH,10Z D=0.120IN,L=0.300IN, I=385MA
L502 L504 L506 L508	CHOKE,CHIP,1UH TAPE AND REEL
L510	CHOKE,COATED,820UH 10Z,D=0.120IN L=0.300IN,I=29MA
Q501 Q502 Q503 Q506	NPN,TO-37,AMP F=9G,V=10,ICBO=1.0uA P=250mW,HFE=100,SS#2
Q504	NPN,TO-35,AMP F=9G,V=10,ICBO=1.0uA P=290mW,HFE=100,SS#2
Q505 Q507	NPN,317-0112,H Freq F=3G,V=10,Ices=1mA P=2W,hFE=200,SS#2
Q515	NPN,SOT-23,MED PWR F=250M,V=40,Icbo=10N P=310m,hFE=40,SS#2
SCH	SCH,VCO BD,2500

WAVETEK PARTS LIST | OSCILLATOR BD,2500

-PART-NO	MFGR	WAVETEK NO.	QTY
HYBRID-KT	W-I	1219-00-0629	1.000
	JEF	1810-03-0010	14.000
02-CC	CLCFT	1816-00-0102	4.000
	JEF	1810-03-0821	1.000
	NEC	4902-68-1370	4.000
	NEC	4902-68-1350	1.000
	NOT	4902-00-5590	2.000
1-23	SIEM	4902-00-0170	1.000
355	W-I	0014-30-0355	1.000

1218-00-2290	J
PAGE: 2	REV

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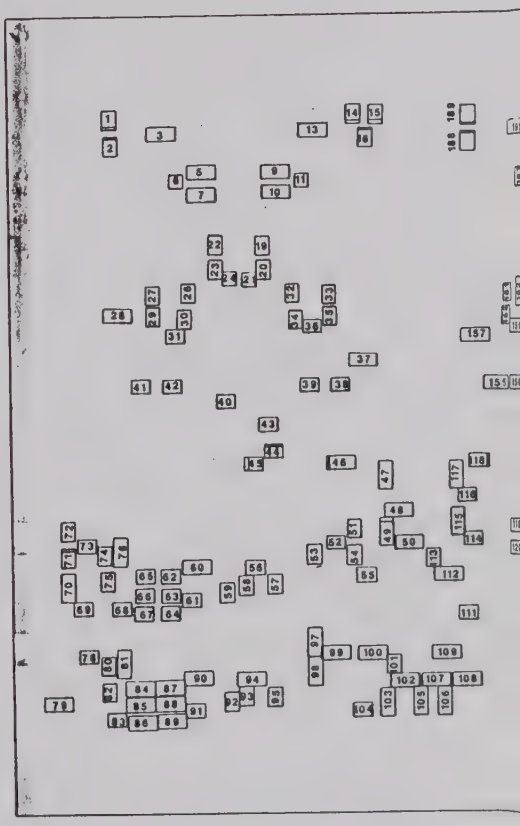
REF DES.	LAYOUT #
C501	178
C502	38
C503	155
C504	41
C505	138
C506	142
C507	140
C508	144
C509	139
C510	143
C511	141
C512	145
C513	219
C514	Side 2
C515	Side 2
C516	Side 2
C517	Side 2
C518	Side 2
C519	212
C520	Side 2
C521	Side 2
C522	Side 2
C523	Side 2
C524	221
C525	222
C526	216
C527	206
C528	263
C529	Side 2
C530	185
C531	186
C532	Side 2
C533	173
C534	174
C535	166
C536	Side 2
C537	153
C538	Side 2
C539	176
C540	11
C541	10
C542	Side 2
C543	33
C544	35
C545	21
C546	258
C548	43
C548	Side 2
C549	36
C550	181
C551	183
C552	Side 2
C553	161
C554	158
C555	165
C556	265
C557	152
C558	Side 2
C559	159
C560	6
C561	7
C562	Side 2
C563	27
C564	29
C565	24
C566	267
C567	40
C568	Side 2
C569	31
C570	116
C571	114
C572	47
C573	93
C574	Not Used
C575	52
C576	Not Used
C577	51
C578	73
C579	106
C580	105
C581	103
C582	111
C583	113
C584	Not Used
C585	99
C586	61
C587	95
C588	97
C589	78
C590	75
C591	Side 2
C592	Not Used
C593	Not Used
C594	Not Used
C595	Not Used
C596	Not Used
C597	Side 2
C598	Not Used
C599	Not Used
C600	Not Used
C601	Not Used
C602	Not Used
C603	Not Used
C604	Not Used
C605	Not Used
C606	Not Used
C607	Not Used
C608	Not Used
C609	Not Used
C610	Not Used
C611	Not Used
C612	Not Used
C613	Not Used
C614	Not Used
C615	Not Used
C616	Not Used
C617	Side 2
C618	Side 2
C619	Side 2
C620	243
C621	Side 2
C622	Side 2
C623	Side 2
C624	Side 2
C625	Side 2
C626	Side 2
C627	Not Used
C628	Side 2
C629	270
C630	132
C631	120
C632	119
C633	122
C634	68
C635	104
C636	55
C637	58
C638	57
C639	69
C640	125
C641	91
C642	83
C643	82
C644	255
C645	256
C646	220
C647	204
C648	253
C649	261
L509	Not Used
L510	Side 2
L511	101
L512	Not Used
L513	Side 2
L514	80
L515	Not Used
L516	Not Used
L517	Not Used
L518	Not Used
L519	Not Used
L520	Not Used

L521	Side 2	R541	174	R595	Not Used	R649	64
L522	Side 2	R542	177	R596	Not Used	R650	67
L523	Side 2	R543	9	R597	Not Used	R651	87
L524	Side 2	R544	19	R598	Not Used	R652	84
L525	Side 2	R545	37	R599	Not Used	R653	88
L526	Side 2	R546	20	R600	Not Used	R654	85
L527	74	R547	32	R601	Not Used	R655	89
L528	Side 2	R548	34	R602	Not Used	R656	86
L529	Not Used	R549	39	R603	Not Used	R657	81
L530	72	R550	182	R604	Not Used	R658	126
L531	Side 2	R551	168	R605	Not Used	R659	231
L532	Side 2	R552	164	R606	Not Used	R660	200
L533	Not Used	R553	157	R607	Not Used	R661	217
		R554	162	R608	Not Used	R662	128
R501	Not Used	R555	48	R609	123	R663	130
R502	Not Used	R556	160	R610	124	R664	79
R503	Not Used	R557	156	R611	233	R665	223
R504	137	R558	5	R612	235	R666	225
R505	131	R559	22	R613	229	R667	221
R506	135	R560	23	R614	228	R668	222
R507	134	R561	28	R615	90	R669	232
R508	136	R562	26	R616	234	R670	238
R509	208	R563	30	R617	237	R671	240
R510	203	R564	42	R618	239	R672	271
R511	Not Used	R565	54	R619	238	R673	
R512	207	R566	53	R620	236		
R513	202	R567	129	R621	224	CR501	249
R514	247	R568	76	R622	Not Used	CR502	251
R515	248	R569	Not Used	R623	50	CR503	Side 2
R516	252	R570	Not Used	R624	146	CR504	244
R517	250	R571	70	R625	147	CR505	Side 2
R518	241	R572	108	R626	148	CR506	195
R519	242	R573	107	R627	149	CR507	197
R520	245	R574	102	R628	150	CR508	194
R521	246	R575	109	R629	117	CR509	196
R522	213	R576	100	R630	115	CR510	14
R523	214	R577	112	R631	268	CR511	15
R524	209	R578	133	R632	269	CR512	16
R525	210	R579	121	R633	264	CR513	Side 2
R526	211	R580	56	R634	257	CR514	189
R527	198	R581	40	R635	254	CR515	188
R528	199	R582	94	R636	Not Used	CR516	1
R529	223	R583	98	R637	260	CR517	2
R530	201	R584	Not Used	R638	259	CR518	154
R531	218	R585	Not Used	R639	262	CR519	44
R532	215	R586	Not Used	R640	193	CR520	151
R533	205	R587	Not Used	R641	13	CR521	45
R534	246	R588	Not Used	R642	191	CR522	Not Us
R535	184	R589	Not Used	R643	3	CR523	227
R536	169	R590	Not Used	R644	Not Used	CR524	225
R537	167	R591	Not Used	R645	62	CR525	Side 2
R538	179	R592	Not Used	R646	65	CR526	Side 2
R539	171	R593	Not Used	R647	63	CR527	Side 2
R540	172	R594	Not Used	R648	66	CR528	Side 2
						CR529	46
						CR530	118
						CR531	49
						CR532	127
						CR533	71



NOTE UNLESS OTHERWISE SPECIFIED

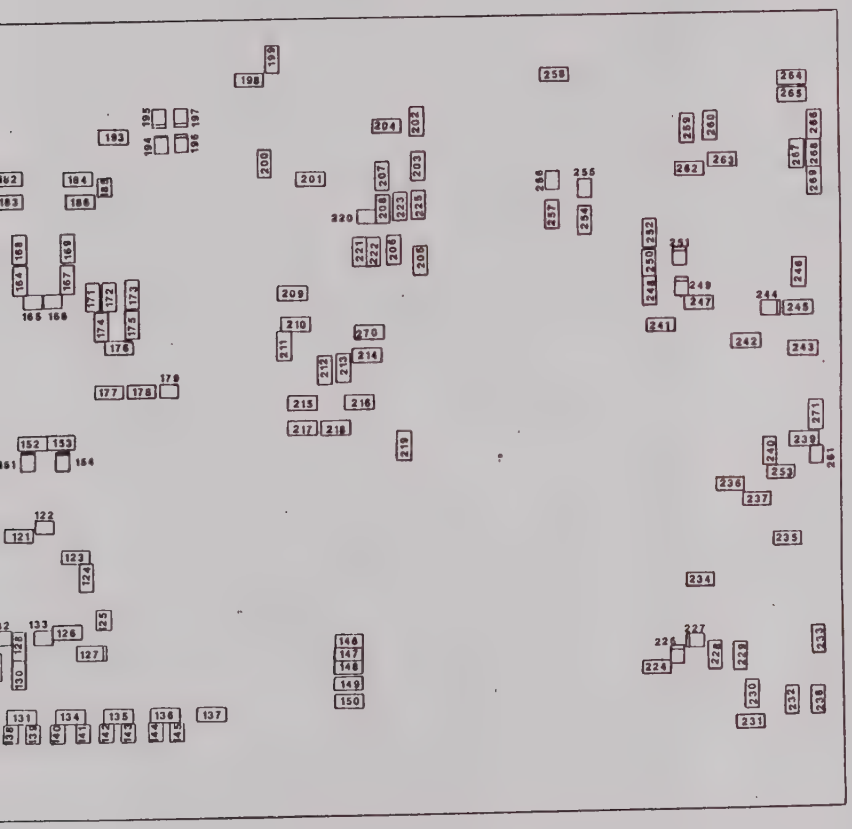


FIGURE 10-8A1

REV	ECN	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN C. KEISER	DATE 6-87	WAVETEK
MATERIAL	PROJ ENGR		TITLE OSCILLATOR BD. SIDE 1
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG		MODEL NO 2500 / DWG NO 0012-20-0052 / REV D
	SCALE NTS		CODE IDENT 34280 / SHEET / OF 3

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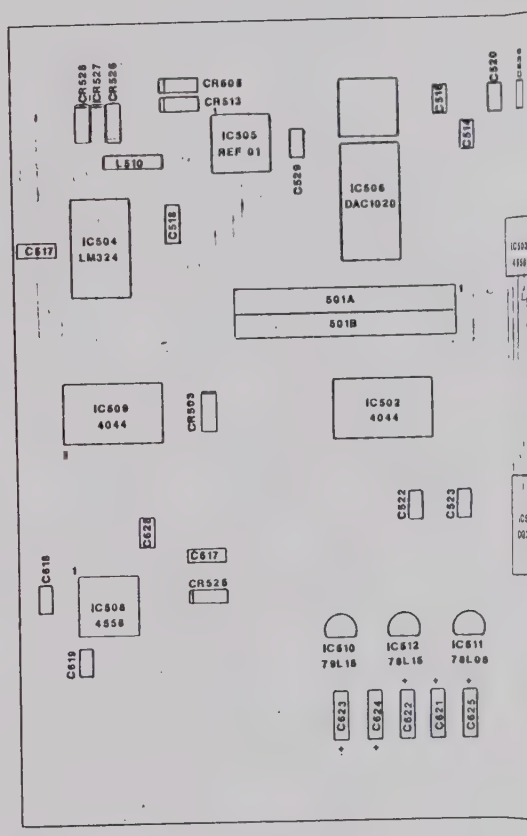

NOTE UNLESS OTHERWISE SPECIFIED

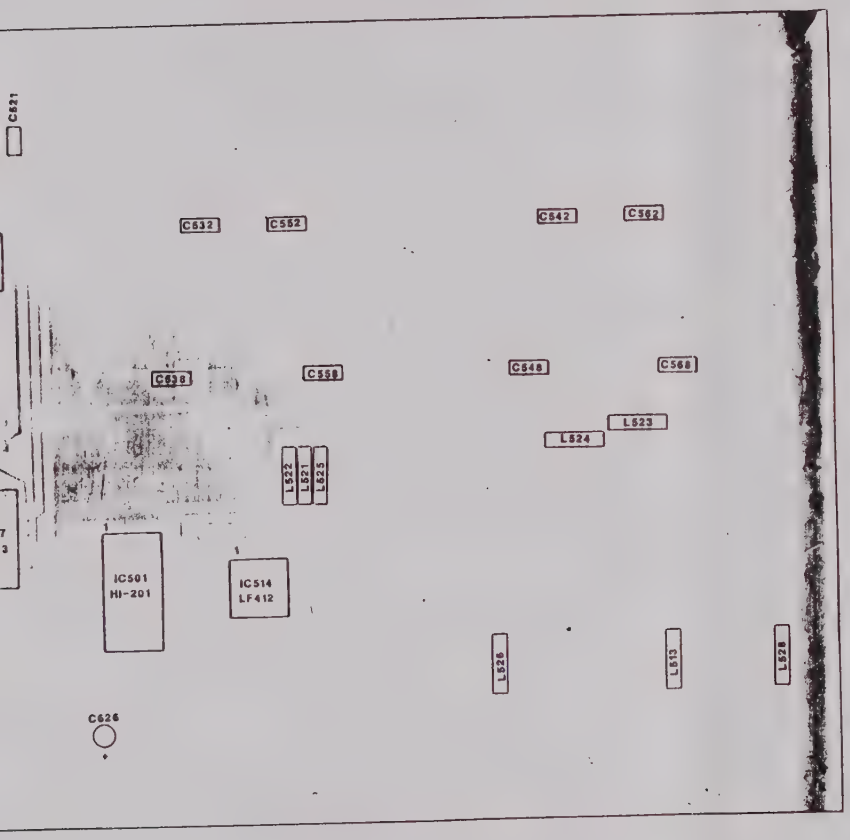

FIGURE 10-8A2

REV	ECN	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN C. KEISER	DATE 6-87	WAVETEK
MATERIAL	PROJ ENGR		TITLE OSCILLATOR BD. (SIDE 2)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG		MODEL NO 2500 / DWG NO 0012-20-0052 / REV D
	SCALE		CODE IDENT 34280 / SHEET 2 OF 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
C501 C502 C503 C504 C505 C506 C507 C508 C509 C510 C511 C512 C524 C525 C530 C531 C539 C540 C541 C549 C550 C551 C559 C560 C561 C569 C570 C571 C572 C575 C578 C579 C580 C581 C582 C583 C585 C586 C587 C589 C590 C633 C634 C635 C636 C638 C639 C641 C642 C643 C646 C647 C648 C699	CAP,CER,1000PF,100V 20%,CHP,X7R ,08"X.05",T/R	145-006	W-I	1510-00-9102	54.000
C513 C519 C620 C629	CAP,CER,.15UF,50V 20%,CHP,X7R ,12"X.10",T/R	1209B154M500	NOVA	1510-05-3154	4.000
C526 C527 C528 C573 C631 C637 C640 C644 C645	CAP,CHIP,.01 UF TAPE AND REEL	C0805C103K5RAC	UNCAR	1510-02-6103	9.000
C533	CAP,CHIP,33 PF	MA18330J	MURGA	1510-02-8330	1.000
C534	CAP,CHIP,39 PF	MA18390J	MURGA	1510-02-8390	1.000
C535 C537	CAP,CHIP,39 PF	C0805C390J5GAH	UNCAR	1510-01-5390	2.000
C543	CAP,CHIP,30 PF	MA18300J	MURGA	1510-02-8300	1.000
C544 C553	CAP,CHIP,22 PF	MA18220J	MURGA	1510-02-8220	2.000
C545 C547	CAP,CHIP,33 PF TAPE AND REEL	C0805C330J5GAH	UNCAR	1510-01-5330	2.000
C546 C555 C557	CAP,CHIP,27 PF TAPE AND REEL	C0805C270J5GAH	UNCAR	1510-01-5270	3.000
C554	CAP,CHIP,20 PF	MA18200J	MURGA	1510-02-8200	1.000
C556 C566 C630 C632	CAP,CER,.1UF,50V 10%,CHP,X7R ,12"X.10" T/R	51C1209-B104Z	CFI	1510-00-3104	4.000
C563 C564	CAP,CHIP,15 PF	MA18150J	MURGA	1510-02-8150	2.000
C565 C567	CAP,CHIP,15 PF	C0805C150J5GAH	UNCAR	1510-01-5150	2.000
C577 C588	CAP,CHIP,12 PF TAPE AND REEL	C0805C120J5GAH	UNCAR	1510-01-5120	2.000
CR501 CR502 CR504 CR523 CR524	DIODE,PLANAR,HI SPD SWIT,SOT-23,V=75,IO= 250m,SUR I=250m,SS12	BAS16	APX	4812-02-0005	5.000
CR506 CR507 CR508 CR509 CR510 CR511 CR512 CR514 CR515 CR516 CR517	DIODE,VAR CAP SOT-23,V=28,IO=20mA CT=1.8pF,SS12	BBY31 (SOT-23)	APX	4807-02-0005	11.000
CR518 CR519 CR520 CR521 CR529 CR530 CR531	DIODE,PIN,GP DO5-07,V=100V CJ=0.4pF,SS12	AL67226-07	EATON	4805-02-0016	7.000
CR532 CR533	DIODE,HOT CAR,SOT-23 SMD,V=4VCT=1pF,SS11	MMBD101	MOT	4809-02-0015	2.000

WAVETEK PARTS LIST	HYBRID PI KT,USC BD, 2500	1219-00-0629 PAGE: 1	A REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG
L511 L527 L530	CHOKE,CHIP,1UH TAPE AND REEL	1000
L514	CHOKE,CHIP,.1 UH TAPE AND REEL	SS103
Q513 Q514	PNP,SOT-23,MED PWR F=200M,V=40,Icbo=10n P=350m,hFE=40,SS12	MSSB0
R504	RES,CH,1/8W,5%,150	ERJ-8
R505 R506 R507 R508 R518 R520 R529 R534 R618 R629 R630 R665 R666	RES,CH,1/8W,5%,1000	ERJ-8
R509 R510 R512 R513	RES,CH,1/8W,5%,82K	RMC 1
R514 R516 R614 R663	RES,CH,1/8W,5%,100K	ERJ8G
R515 R517 R621 R658 R662	RES,CH,1/8W,5%,330K	RMC 1
R519 R521 R578 R579 R609 R610 R659	RES,CH,1/8W,5%,10000	ERJ-8
R522 R525	RES,CHIP,1/8W,5%,12K	ERJ-8
R523	RES,CH,1/8W,1%,1000	RCK10
R524 R581 R615 R617 R618	RES,CH,1/8W,1%,6.80K	RMC 1
R526 R634 R635 R667 R668 R669 R670	RES,CH,1/8W,5%,6.2M	RMC 1
R527	RES,CH,1/8W,1%240OHM	RMC 1
R528	RES,CH,1/8W,1%,10	RMC 1
R530 R568 R657	RES,CH,1/8W,5%,200	ERJ-M
R531	RES,CH,1/8W,1%,2.7K	RMC 1
R532	CHIP RES., 432 OHM 1/8 W, 1%	RMC 1
R533 R661	RES,CH,1/8W,1%,2K	RMC 1
R535 R543 R550 R558 R645 R646 R647 R648 R649 R650	RES,CH,1/8W,5%,300	ERJ-8
R536	RES,CH,1/8W,5%,27	ERJ-8
R537	RES,CH,1/8W,5%,24	ERJ-8
R538 R545	RES,CH,1/8W,5%,100	ERJ-8
R539 R540	RES,CH,1/8W,5%,15	ERJ-8
R541 R548 R556 R563	RES,CH,1/8W,5%,330	ERJ-8
R542 R549 R557 R564	RES,CH,1/8W,5%,390	ERJ-8
R544 R551 R559 R623	RES,CH,1/8W,5%,39	ERJ-8

WAVETEK PARTS LIST | HYBRID PI KT,USC BD, 2500

FGR-PART-NO	MFGR	WAVETEK NO.	QTY
G-102-CC	CLCFT	1816-00-0102	3.000
01	CLCFT	1816-00-1008	1.000
(SOT-23)	SIEM	4902-00-0800	2.000
CJ151D	PNSNC	4711-05-1509	1.000
CJ102D	PNSNC	4711-05-1001	13.000
08235C	KMYO	4711-05-8202	4.000
0104D	PNSNC	4711-05-1003	4.000
03345C	KMYO	4711-05-3303	5.000
CJ103D	PNSNC	4711-05-1002	7.000
CJ-123D	PNSNC	4711-05-1202	2.000
FB	A-B	4711-03-1001	1.000
8011C	KMYO	4711-03-6801	5.000
6255C	KMYO	4711-05-6204	7.000
4091C	KMYO	4711-03-2400	1.000
0081C	KMYO	4711-03-1009	1.000
J201D	PNSNC	4711-05-2000	3.000
7011C	KMYO	4711-03-2701	1.000
3291C	KMYO	4711-03-4320	1.000
0011C	KMYO	4711-03-2001	2.000
J301D	PNSNC	4711-05-3000	10.000
J270D	PNSNC	4711-05-2709	1.000
J240D	PNSNC	4711-05-2409	1.000
J101D	PNSNC	4711-05-1000	2.000
J150D	PNSNC	4711-05-1509	2.000
J331D	PNSNC	4711-05-3300	4.000
J391D	PNSNC	4711-05-3909	4.000
J390D	PNSNC	4711-05-3909	4.000

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
R546 R547 R552 R554 R560 R562 R674	RES,CH,1/8W,5%,11	ERJ-8GCJ110D	PNSNC	4711-05-1109	7.000
R553	RES,CH,1/8W,5%,430	ERJ-8GCJ43A0	PNSNC	4711-05-4300	1.000
R555 R567	RES,CH,1/8W,5%,240	ERJ-8GCJ241D	PNSNC	4711-05-2400	2.000
R561 R639	RES,CH,1/8W,5%,560	ERJ-8GCJ561D	PNSNC	4711-05-5600	2.000
R565	RES,CH,1/8W,5%,470	ERJ-8GCJ471D	PNSNC	4711-05-4700	1.000
R566 R583	RES,CH,1/8W,5%,2200	ERJ-8GCJ222D	PNSNC	4711-05-2201	2.000
R571	RES,CH,1/8W,5%,51	ERJ-8GCJ510D	PNSNC	4711-05-5109	1.000
R572 R573 R574 R611	RES,CH,1/8W,5%,180	ERJ-8GCJ181D	PNSNC	4711-05-1800	4.000
R575	RES,CH,1/8W,5%,82	ERJ-8GCJ820D	PNSNC	4711-05-8209	1.000
R576	RES,CH,1/8W,5%,10	ERJ-8GCJ100D	PNSNC	4711-05-1009	1.000
R577	RES,CH,1/8W,5%,30K	RMC 1803035C	KMYO	4711-05-3002	1.000
R580 R612 R620	RES,CH,1/8W,5%,3000	ERJ-8GCJ302D	PNSNC	4711-05-3001	3.000
R582	RES,CH,1/8W,5%,4.7K	ERJ-8GCJ472D	PNSNC	4711-05-4701	1.000
R613	RES,CH,1/8W,5%,180K	RMC 1801845C	KMYO	4711-05-1803	1.000
R624 R625 R626 R627 R628 R660	RES,CH,1/8W,5%,1201	ERJ-8GCJ122D	PNSNC	4711-05-1201	6.000
R631 R632 R633	RES,CH,1/8W,5%,270K	RMC 1802745C	KMYO	4711-05-2703	3.000
R637 R638 R664	RES,CH,1/8W,5%,15K	RMC 1801535C	KMYO	4711-05-1502	3.000
R640 R641 R642 R643 R671 R672	RES,CH,1/8W,5%,1500	ERJ-8GCJ152D	PNSNC	4711-05-1501	6.000
R651 R652 R653 R654 R655 R656	RES,CH,1/8W,5%,270	ERJ-8GCJ271D	PNSNC	4711-05-2700	6.000
R673	TRM,CM,L,5K,10Z,SM 1T,PN,CW,.22H,.25W .312L,TA	3325P-1-502	BOU	4610-70-1502	1.000

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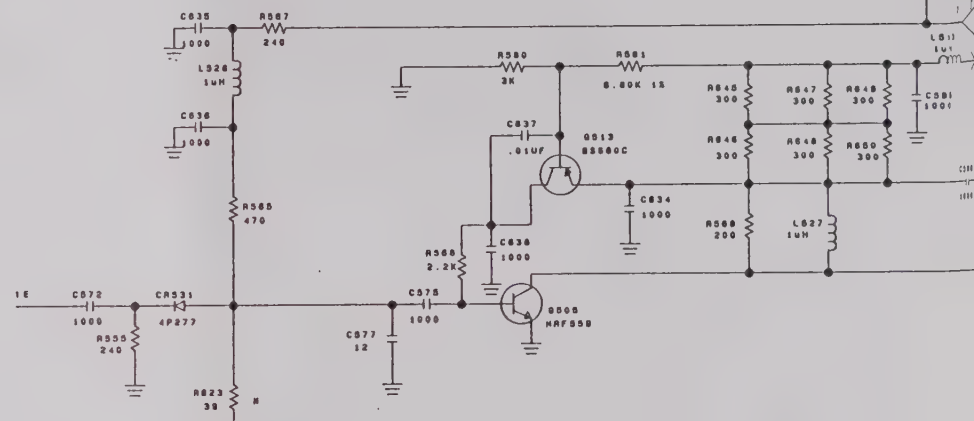

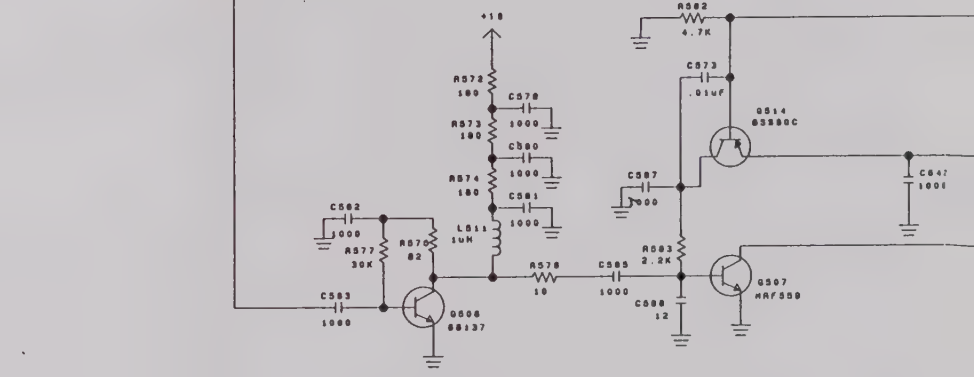

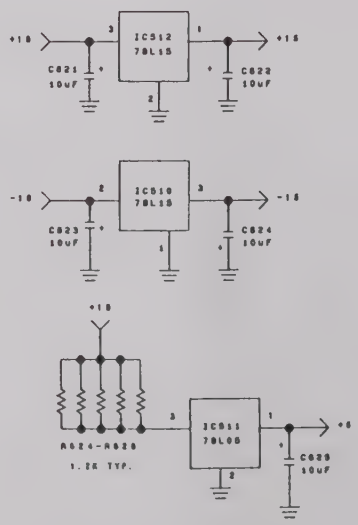

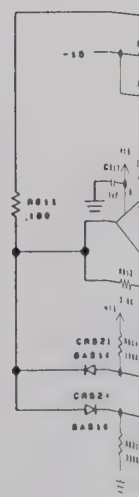

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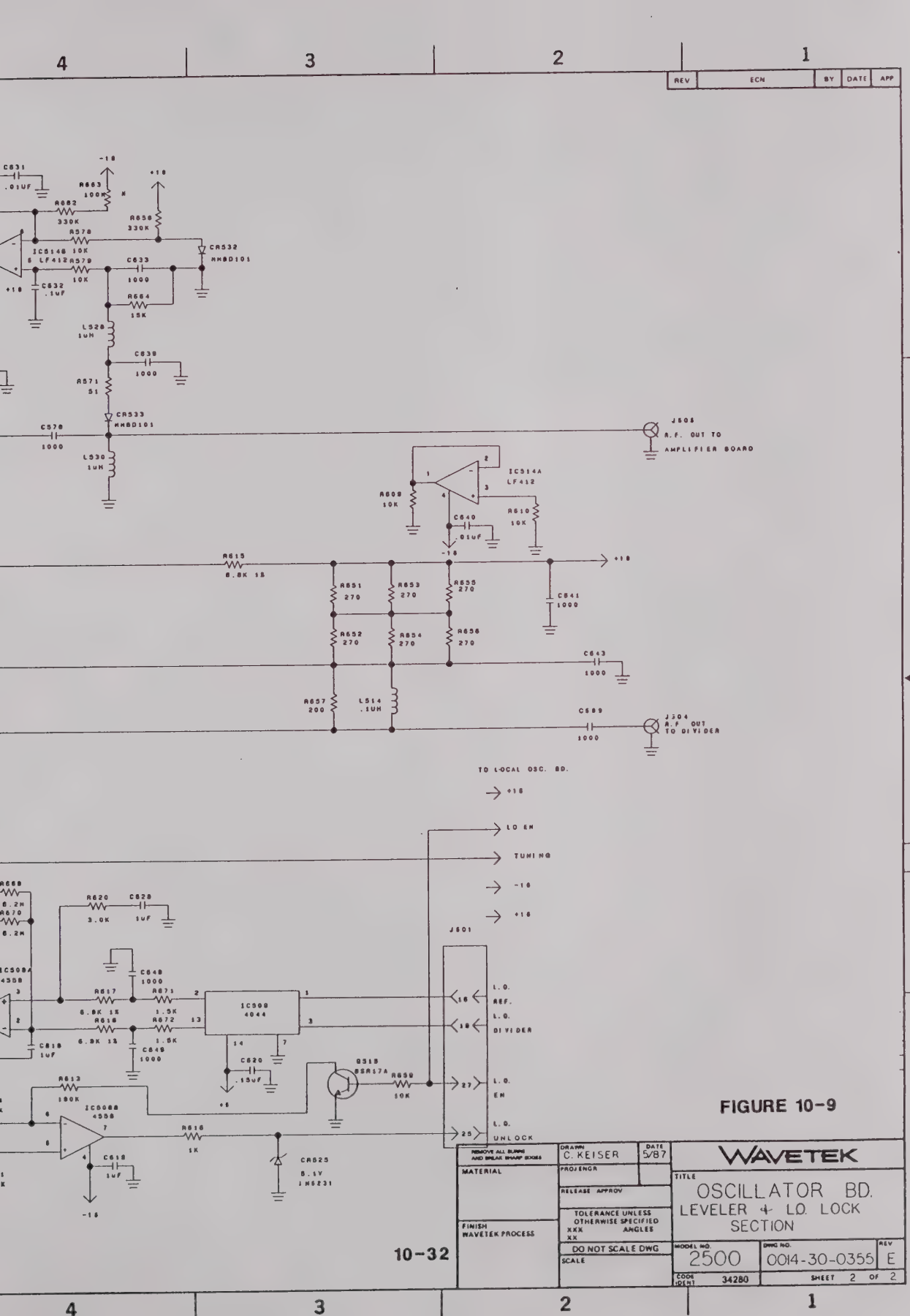
REV
ECN
BY
DATE
APP
C631 .01UF
R683 100K
R682 330K
R658 330K
R578 10K
IC5148 LF412
R579 10K
C632 .1UF
C633 1000
R664 15K
CR532 MMBD101
L528 1UH
C638 1000
R571 51
CR533 MMBD101
C578 1000
L530 1UH
J505 A.F. OUT TO AMPLIFIER BOARD
IC5144 LF412
R608 10K
C640 .01UF
R610 10K
R615 8.8K 1%
R651 270
R653 270
R655 270
C641 1000
R652 270
R654 270
R656 270
C643 1000
R657 200
L514 .1UH
C589 1000
J504 A.F. OUT TO DIVIDER
TO LOCAL OSC. BD.
+18
LO EN
TUNING
-18
+18
J501
R668 8.2M
R670 8.2M
R620 3.0K
C628 1UF
IC5084 4558
C648 1000
R617 6.8K 1%
R671 1.5K
IC5088 4044
R618 6.8K 1%
R672 1.5K
C649 1000
C619 1UF
C620 .15UF
Q518 BSR17A
R659 10K
R613 180K
IC5088 4558
R616 1K
C618 1UF
CR525 5.1V 1N5231
L.O. REF.
L.O. DIVIDER
L.O. EN
L.O. UNLOCK
FIGURE 10-9
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN C. KEISER
DATE 5/87
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX
DO NOT SCALE DWG
SCALE
WAVETEK
TITLE
OSCILLATOR BD. LEVELER & LO. LOCK SECTION
MODEL NO. 2500
DWG NO. 0014-30-0355
REV E
CODE IDENT 34280
SHEET 2 OF 2
10-32

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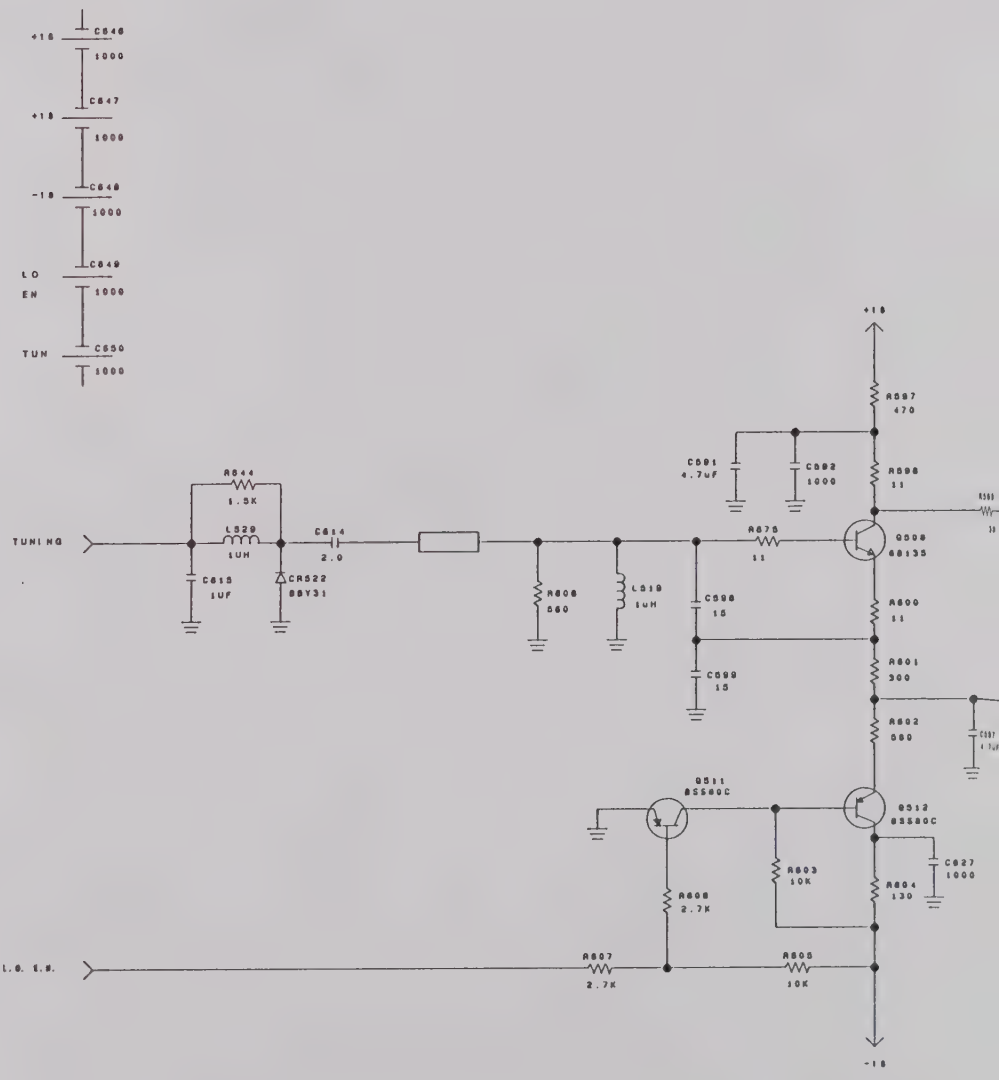


NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP
F	1111	CK	5/87	

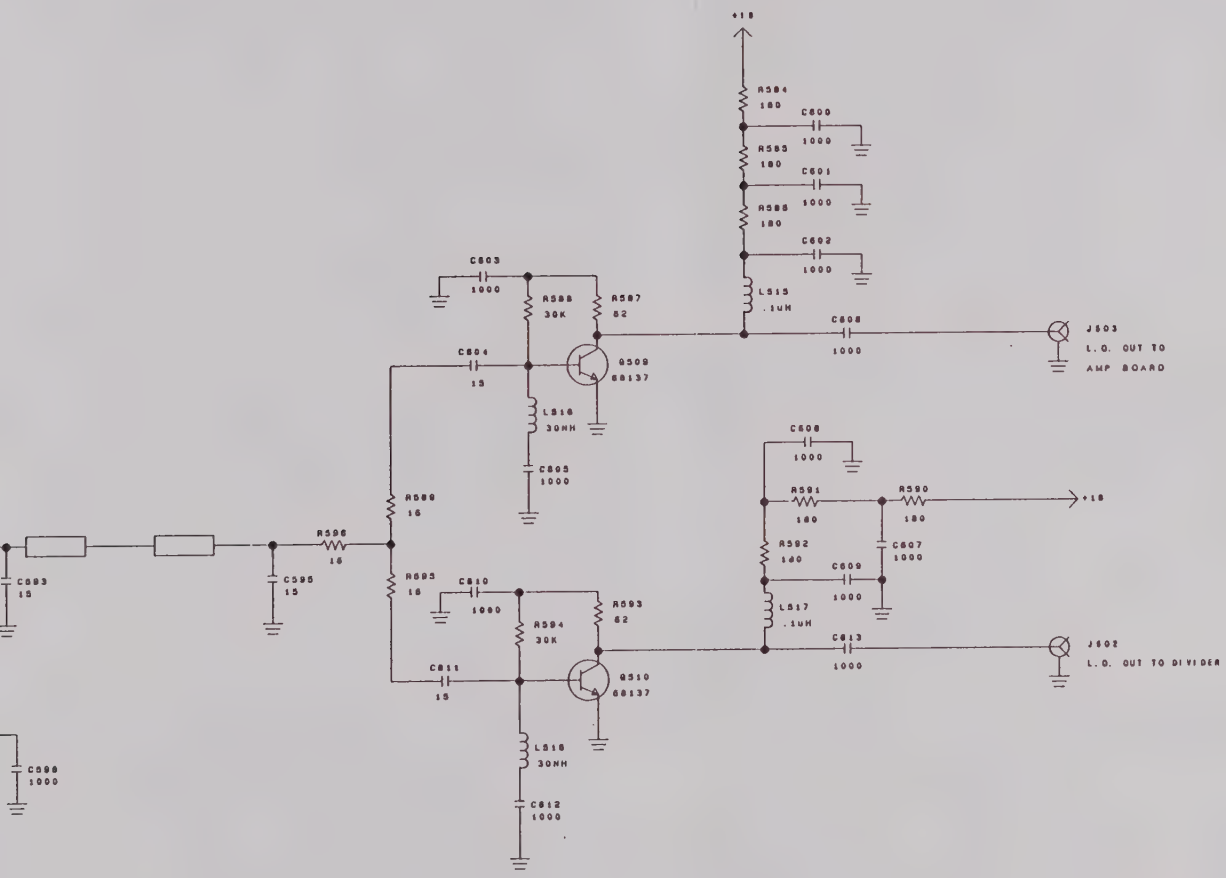
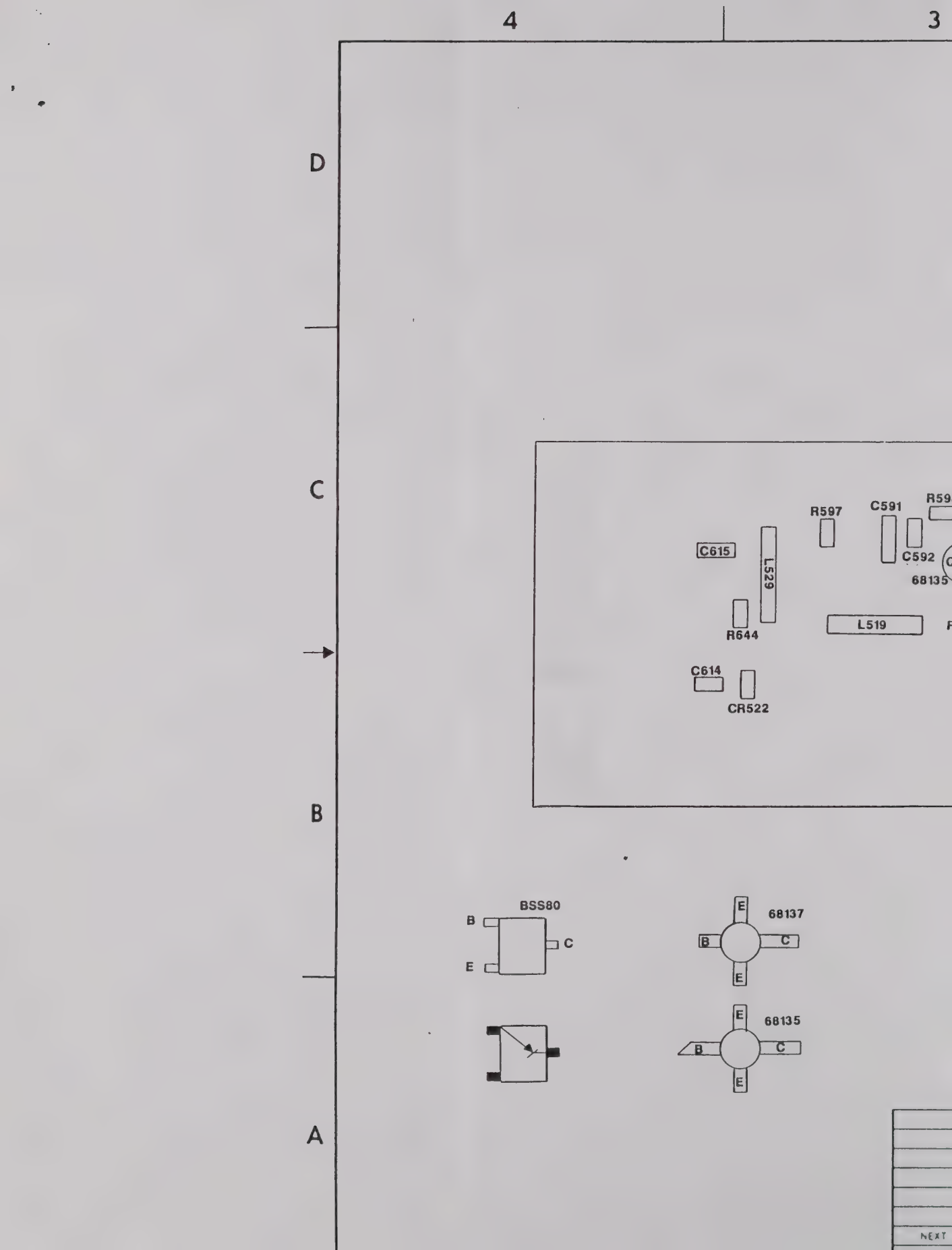


FIGURE 10-10

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN K. KEISER	DATE 5/87	WAVETEK
MATERIAL	PROJ ENGR		TITLE LOCAL OSCILLATOR BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG		MODEL NO 2500 / DWG NO CC14-30-0371 / REV B
	SCALE		CODE IDENT 34280 / SHEET 1 OF 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
C591 C597	CAP,MON,50V,4.7UF	SR505E475MAA	AER	1510-11-3475	2.000
C615	CAP,MON,50V,1UF	3420-050-E105M	AER	1510-11-3105	1.000
KIT	HYBRID PTS KT,LOCAL OSC BD,2500	2500-LOC-OSC-HYBD-KT	W-I	1219-00-0631	1.000
L519	CHOKE,CHIP,1UH TAPE AND REEL	1008 CS-102-CC	CLCFT	1816-00-0102	1.000
L529	CHOKE,COATED,1UH,10% D=0.120IN,L=0.300IN, I=385MA	08N1RO	JEF	1810-03-0010	1.000
Q508	NPN,TO-35,AMP F=9G,V=10,JCBO=1.0uA P=290mW,HFE=100,SS#2	NE68135	NEC	4902-68-1350	1.000
Q509 Q510	NPN,TO-37,AMP F=9G,V=10,JCBO=1.0uA P=250mW,HFE=100,SS#2	NE68137	NEC	4902-68-1370	2.000
SCH	SCH,LOCAL OSC,2500	0014-30-0371	W-I	0014-30-0371	1.000

WAVETEK PARTS LIST	LOCAL OSC BD, 2500	1218-00-2590 PAGE: 1	D REV


4
3
D
C
B
A
R597
C591
R59
C615
L529
C592
68135
R644
L519
C614
CR522
BSS80
B
C
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68137
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B
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68135
E
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E
NEXT

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APP

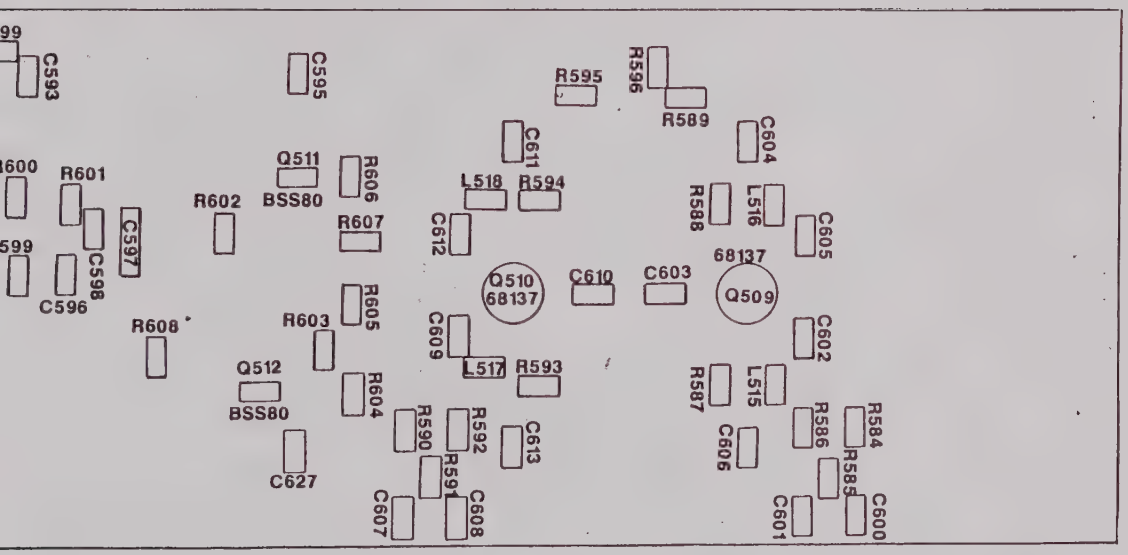


FIGURE 10-10A

	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS . DECIMALS XX . XXX . ANGLES ±

CONTRACT NO

APPROVALS	DATE
DRAWN C. KEISER	6-87
CHECKED	

MATERIAL

FINISH

DO NOT SCALE DRAWING

10-36

WAVETEK INDIANA, INC.

2500
LOCAL OSC. BOARD

SIZE	CODE IDENT NO	DRAWING NO.
C	34280	0012-20-0051

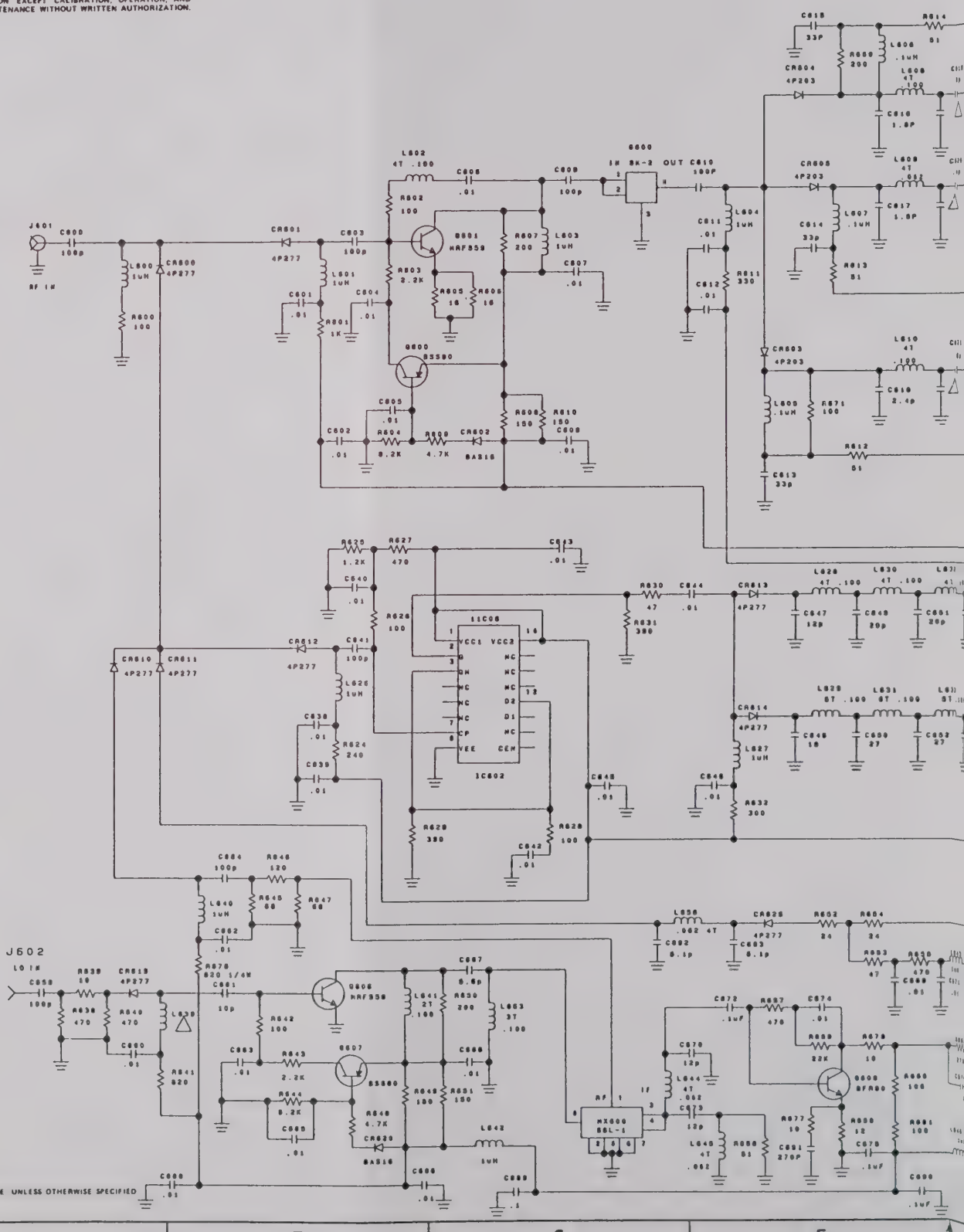
SCALE NTS SHEET 1 OF 1

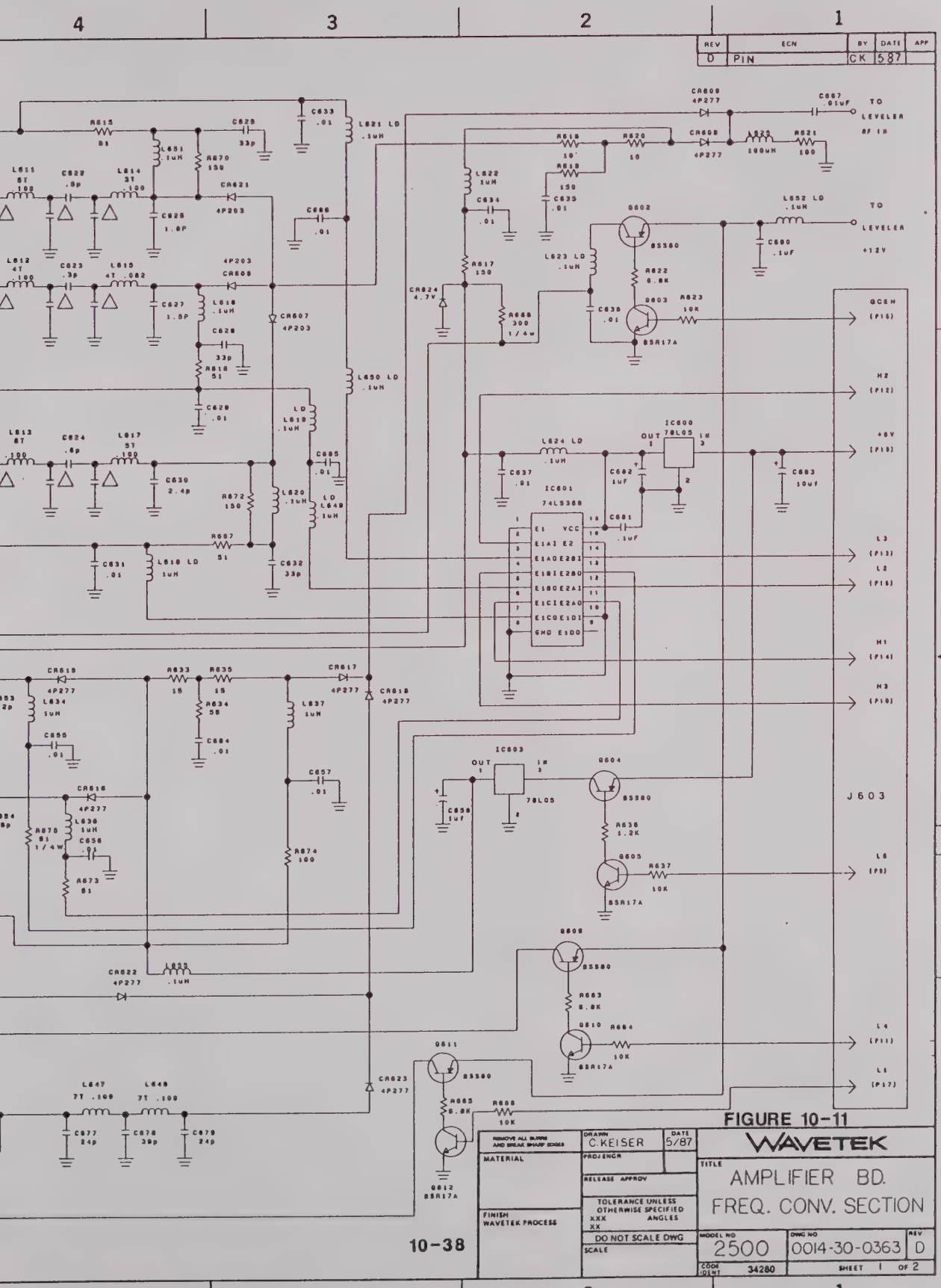
USED ON

CATION

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

△ MICROSTRIP COMPONENT




4
3
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5/87
TO LEVELER RF IN
TO LEVELER +12V
IC600 78L05
IC601 74LS368
IC603 78L05
Q602 Q603 Q604 Q605 Q609 Q610 Q611 Q612 2SA1708
J603
FIGURE 10-11
WAVETEK
AMPLIFIER BD.
FREQ. CONV. SECTION
DRAWN C.KEISER
DATE 5/87
MATERIAL
PROJECT
RELEASE APPROV
FINISH WAVETEK PROCESS
TOLERANCE UNLESS OTHERWISE SPECIFIED
DO NOT SCALE DWG
SCALE
MODEL NO 2500
DWG NO 0014-30-0363
REV D
CODE IDENT 34280
SHEET 1 OF 2
10-38

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
C592 C598 C600 C601 C602 C603 C605 C606 C607 C608 C609 C610 C612 C613 C627	CAP,CER,1000PF,100V 20%,CHP,X7R .08"X.05",T/R	145-006	W-I	1510-00-9102	15.000
C593 C595 C604 C611	CAP,CHIP,15 PF	C0805C150J5GAN	UNCAR	1510-01-5150	4.000
C596 C599	CAP,CHIP,15 PF	MA18150J	MURGA	1510-02-8150	2.000
C614	CAP,CHIP,2.0 PF	MA18R20B	MURGA	1510-02-8209	1.000
CR522	DIODE,VAR CAP SOT-23,V=28,ID=20mA CT=1.8pF,SS#2	MBV31 (SOT-23)	MPX	4807-02-0005	1.000
L515 L517	CHOKE,CHIP,.1 UH TAPE AND REEL	SS163-01	CLCFT	1816-00-1008	2.000
L516 L518	CHOKE,CHIP,30NH TAPE AND REEL	1008 CT-300-CC	CLCFT	1816-00-0300	2.000
Q511 Q512	PNP,SOT-23,MED PWR F=200M,V=40,Icbo=10n P=350m,hFE=40,SS#2	BSS60C (SOT-23)	SIEM	4902-00-0800	2.000
R584 R585 R586 R590 R591 R592	RES,CH,1/8W,5%,180	ERJ-8GCJ181D	PNSNC	4711-05-1800	6.000
R587 R593	RES,CH,1/8W,5%,62	ERJ-8GCJ620D	PNSNC	4711-05-6209	2.000
R588 R594	RES,CH,1/8W,5%,30K	RMC 1803035C	KMYO	4711-05-3002	2.000
R589 R595 R596	RES,CH,1/8W,5%,16	ERJ-8GCJ160D	PNSNC	4711-05-1609	3.000
R597	RES,CH,1/8W,5%,470	ERJ-8GCJ471D	PNSNC	4711-05-4700	1.000
R598 R600 R675	RES,CH,1/8W,5%,11	ERJ-8GCJ110D	PNSNC	4711-05-1109	3.000
R599	RES,CH,1/8W,5%,39	ERJ-8GCJ390D	PNSNC	4711-05-3909	1.000
R601	RES,CH,1/8W,5%,300	ERJ-8GCJ301D	PNSNC	4711-05-3000	1.000
R602 R608	RES,CH,1/8W,5%,560	ERJ-8GCJ561D	PNSNC	4711-05-5600	2.000
R603 R605	RES,CH,1/8W,5%,10000	ERJ-8GCJ103D	PNSNC	4711-05-1002	2.000
R604	RES,CH,1/8W,5%,130	ERJ-8GCJ131D	PNSNC	4711-05-1300	1.000
R606 R607	RES,CH,1/8W,5%,2700	ERJ-8GCJ272D	PNSNC	4711-05-2701	2.000
R644	RES,CH,1/8W,5%,1500	ERJ-8GCJ152D	PNSNC	4711-05-1501	1.000

1) R600
2) L600
3) C600
4) CR600+
5) CR601+
6) L601
7) C603
8) R603
9) R602
10) R606
11) R605
12) C604
13) C601
14) R601
15) C602
16) Q600
17) C605
18) R604
19) R609
20) CR602+
21) C608
22) R608
23) R610
24) R607
25) C606
26) C609
27) L603
28) C607
29) C610
30) L604
31) C611
32) R611
33) C612
34) CR603+
35) CR605+
36) CR604+
37) R639
38) L606
39) C615
40) R614
41) C616
42) C619
43) C622
44) C626
45) R670
46) R615
47) C633
48) C625
49) L651
50) C635
51) R619
52) R613
53) R620
54) R6..
55) L622
56) C634
57) CR608+
58) CR609+
59) R621
60) C687
61) J700
62) R77..
63) R731
64) C701
65) R778
66) J702
67) J703
68) J704
69) J709
70) R708
71) C704
72) R705
73) J707
74) C705
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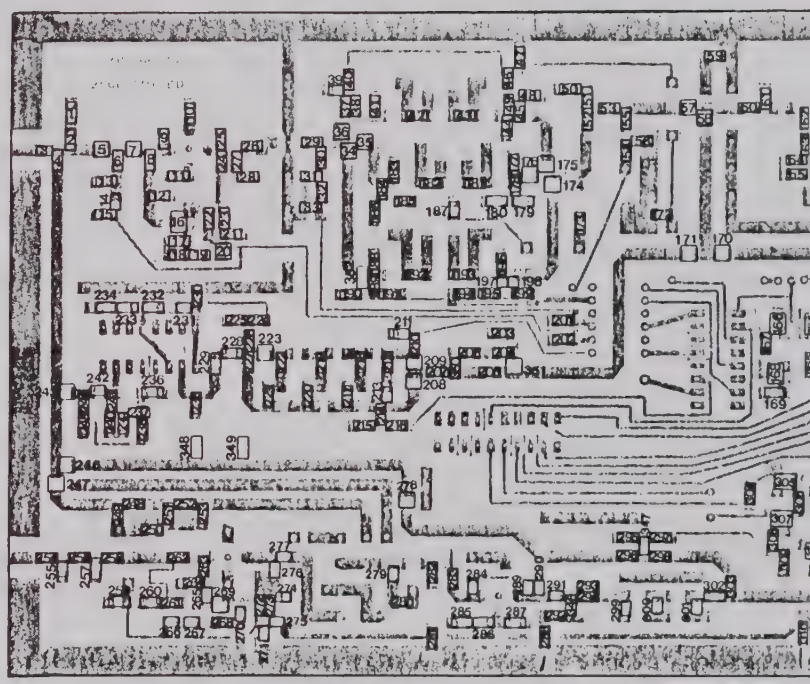
77) R710
78) R780
79) R771
80) C702
81) R714
82) R712
83) C714
84) R715
85) R721
86) R720
87) C711
88) R716
89) R718
90) C712
91) R717
92) C746
93) C713
94) R719
95) C708
96) C710
97) R722
98) R726
99) C716
100) R723
101) R727
102) C715
103) R724
104) R725
105) C718
106) R728
107) R729
108) R735
109) C717
110) R736
111) Q703
112) R731
113) C719
114) R730
115) CR705+
116) C709
117) C721
118) J720
119) C722
120) C727
121) R737
122) C724
123) C723
124) R742
125) R741
126) C745
127) R739
128) C726
129) R740
130) Q705
131) R734
132) R733
133) R732
134) R774
135) R773
136) CR711+
137) CR712+
138) R776
139) R775
140) CR710+
141) R765
142) R764
143) R782
144) R766
145) C735
146) R777
147) R769
148) R772
149) C736
150) C734
151) Q708
152) Q707
153) R711
154) R713
155) R703
156) R783
157) Q701
158) C733
159) C770
160) C707
161) C69..
162) Q60..
163) R636
164) Q605
165) R637
166) R622
167) Q603
169) R623
170) CR618+
171) CR617+
172) C686
173) C685
174) CR607
175) CR621+
176) CR606+
177) C627
178) C616
179) C628
180) R616
181) C623
182) C620
183) C617
184) L607
185) R613
186) C614
187) C629
188) C618
189) L605
190) C613
191) R612
192) C621
193) C624
194) C631
195) C632
196) C630
197) L620
198) R672
199) R667
200) C731
201) C637
202) C636
203) R674
204) C657
205) R635
206) C684
207) R633
208) CR616+
209) CR615+
210) L634
211) C655
212) C653
213) C654
214) L636
215) C656
216) R673
217) C652
218) C651
219) C649
220) C650
221) C648
222) C647
223) CR613+
224) R632
225) C646
226) L627
227) CR614+
228) C644
229) R630
230) C645
231) C643
232) R629
233) R628
234) C642
235) R631
236) C639
237) R627
238) R624
239) C640
240) R625
241) R626
242) C641
243) CR612+
244) L626
245) R638
246) CR611+
247) CR610+
248) C664
249) L640
250) C662
251) R645
252) R...
253) R647
254) C659
255) R638
256) R639
257) L640
258) CR619+
259) C688
260) R641
261) C660
262) C661
263) R642
264) C663
265) R643
266) CR620+
267) R648
268) R644
269) Q607
270) C665
271) C666
272) R649
273) R651
274) C668
275) L642
276) R650
277) C667
278) CR625+
279) C673
280) R655
281) C688
282) C670
283) C672
284) R657
285) C691
286) R677
287) R658
288) C690
289) C674
290) R659
291) R678
292) R661
293) C676
294) R662
295) C669
296) R652
297) R655
298) R654
299) C677
300) C678
301) C679
302) CR623+
303) CR622+
304) R664
305) Q610
306) R663
307) Q609
308) L643
309) C671
310) C675
311) Q611
312) C680
313) R665
314) Q612
315) R644
316) R768
317) C732
318) R763
319) R762
320) CR706+
321) R743
322) R744
323) R745
324) R746
325) C743
326) R747
327) R748
328) C742
329) C744
330) R761
331) R754
332) R755
333) R756
334) R760
335) R758
336) R759
337) R781
338) C728
339) R751
340) R749
341) C729
342) R753
343) R750
344) C730
345) R752
346) R660
347) R653
348) C692
349) C693
350) R634
351) L637
352) R671



NOTE:
REF. #'S 37,45,198,348,349,352. ARE PART OF TECH KIT ASSY.

ZONE	LTR	DESCRIPTION	DATE	APPROVED
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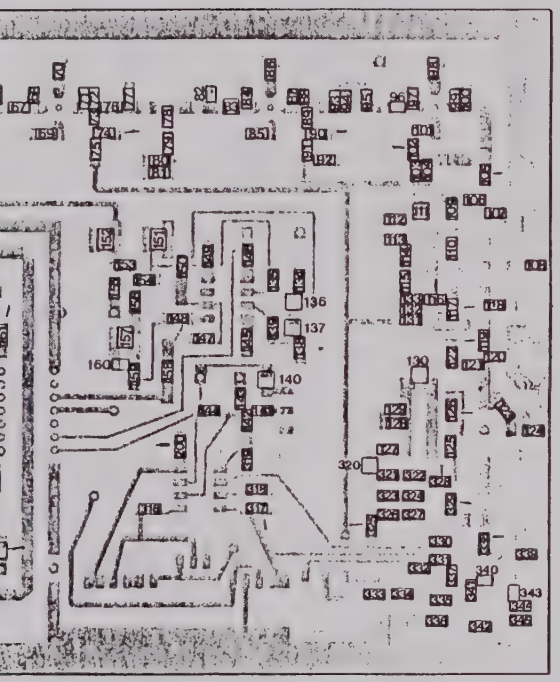

1710-30-0059

FIGURE 10-11A

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN C. KEISER	11-85
CHECKED	

10-39

WAVETEK INDIANA, INC

2500 AMP BOARD (SIDE 1)
PART LAYOUT

SIZE	CODE IDENT NO.	DRAWING NO.
D	34280	0012-30-0035

NEXT ASSY	USED ON
APPLICATION	

SCALE	REV A	SHEET 1 OF 4

4 3 2 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
C600 C603 C609 C610 C641 C659 C664	CAP,CHIP,100 PF TAPE AND REEL	C0805C101J5GAH	UNCAR	1510-01-5101	7.000
C601 C602 C604 C605 C606 C607 C608 C611 C612 C629 C631 C633 C634 C635 C636 C637 C638 C639 C640 C642 C643 C644 C645 C646 C655 C656 C657 C660 C662 C663 C665 C666 C668 C669 C671 C674 C684 C685 C686 C687 C688 C701 C702 C703 C704 C706 C711 C714 C717 C719 C720 C724 C726 C735 C736	CAP,CHIP,.01 UF TAPE AND REEL	C0805C103K5RAL	UNCAR	1510-02-6103	55.000
C613 C614 C615 C625 C628 C632	CAP,CHIP,33 PF TAPE AND REEL	C0805C330J5GAH	UNCAR	1510-01-5330	6.000
C616 C626	CAP,CHIP,1.8 PF	C0805C189D5GAH	UNCAR	1510-01-4189	2.000
C617 C627 C723 C727	CAP,CHIP,1.5 PF TAPE AND REEL	MA181R5B	MURGA	1510-02-8159	4.000
C618 C630	CAP,CHIP,2.4 PF	C0805C249D5GAH	UNCAR	1510-01-4249	2.000
C619 C622	CAP,CHIP,.5 PF	MA180R5B	MURGA	1510-02-8508	2.000
C620	CAP,CHIP,.4 PF	MA180R4B	MURGA	1510-02-8408	1.000
C621 C624	CAP,CHIP,.6 PF	MA180R6B	MURGA	1510-02-8608	2.000
C623	CAP,CHIP,.3 PF	MA180R3B	MURGA	1510-02-8308	1.000
C647 C653 C670 C673	CAP,CHIP,12 PF TAPE AND REEL	C0805C120J5GAH	UNCAR	1510-01-5120	4.000
C648 C654	CAP,CHIP,18 PF	C0805C180J5GAH	UNCAR	1510-01-5180	2.000
C649 C651	CAP,CHIP,20 PF	C0805C200J5GAH	UNCAR	1510-01-5200	2.000
C650 C652	CAP,CHIP,27 PF TAPE AND REEL	C0805C270J5GAH	UNCAR	1510-01-5270	2.000
C661	CAP,CHIP,10 PF	C0805C100J5GAH	UNCAR	1510-01-5100	1.000
C667	CAP,CHIP,5.6 PF	C0805C569D5GAH	UNCAR	1510-01-4569	1.000
C672 C675 C676 C680 C681 C689 C690 C705 C709 C712 C715 C718 C721 C722 C725 C728 C731 C732 C742 C743 C744 C745 C746	CAP,CHIP,.1 MF TAPE AND REEL	CC1210X7R104M050LR	CGW	1510-05-0104	23.000
C677 C679	CAP,CHIP,24 PF	C0805C240J5GAH	UNCAR	1510-01-5240	2.000
C678	CAP,CHIP,39 PF	C0805C390J5GAH	UNCAR	1510-01-5390	1.000
C691	CAP,CHIP,270 PF	C0805C271J5GAH	UNCAR	1510-01-5271	1.000
C707 C716 C729 C730	CAP,CER,1000PF,100V 20%,CHP,X7R .08"X.05",T/R	145-006	W-I	1510-00-9102	4.000

REFERENCE DESIGNATORS	PART DESCRIPTION
C708 C710	CAP,CER,.047PF,50V +80%,-20%,CHP,Y5V .080 "X.05",T/R
C713	CAP,CHIP,8.2 PF
C733 C734	CHIP CAP, 2200 PF
CR600 CR601 CR608 CR609 CR610 CR611 CR612 CR613 CR614 CR615 CR616 CR617 CR618 CR619 CR622 CR623 CR625	DIODE,PIN,GP QDS-07,V=100V CJ=0.4pF,SS#2
CR602 CR620 CR705 CR706 CR710 CR711 CR712	DIODE,PLANAR,HI SPD SWIT,SOT-23,V=75,ID=250m,SUR I=250m,SS#2
CR603 CR604 CR605 CR606 CR607 CR621	DIODE,PIN,POWER SOT-287,V=100V CJ=0.15pF,SS#2
L600 L601 L603 L604 L622 L626 L627 L634 L636 L637 L640 L642 L643	CHOKE,CHIP,10UH TAPE AND REEL
L605 L606 L607 L616 L620 L651	CHOKE,CHIP,.1 UH TAPE AND REEL
Q600 Q602 Q604 Q607 Q609 Q611 Q703 Q705 Q709	PNP,SOT-23,MED PWR F=200M,V=40,Icbo=10n P=350m,hFE=40,SS#2
Q603 Q605 Q610 Q612 Q707 Q708	NPN,SOT-23,MED PWR F=250M,V=40,Icbo=10N P=310m,hFE=40,SS#2
R600 R602 R621 R626 R628 R642 R660 R661 R674 R706 R717	RES,CH,1/8W,5%,100
R601 R703 R775	RES,CH,1/8W,5%,1000
R603 R643 R711 R713 R714 R728 R737 R778	RES,CH,1/8W,5%,2200
R604 R644	RES,CHIP,8.2K
R605 R606	RES,CH,1/8W,5%,16
R607 R650 R707 R718	RES,CH,1/8W,5%,200
R608 R610 R617 R619 R649 R651 R729 R732 R733 R734	RES,CH,1/8W,5%,150
R609 R648 R777	RES,CH,1/8W,5%,4.7K
R611	RES,CH,1/8W,5%,330
R612 R613 R614 R615 R616 R656 R667 R673 R719 R781	RES,CH,1/8W,5%,51
R618 R620 R639 R677 R678 R741 R742	RES,CH,1/8W,5%,10

WAVETEK PARTS LIST | HYBRID PT KT,AMP BD, 2500

G-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
0B05047N50VZY5V1R	NIC	1510-05-1473	2.000
05C8290G5GAH	UNCAR	1510-01-4829	1.000
05C222J5GAC	UNCAR	1510-03-9222	2.000
7226-07	EATON	4805-02-0016	17.000
16	APX	4812-02-0005	7.000
671	MACOM	4805-02-0009	6.000
0 CS-102-CC	CLCFT	1816-00-0102	13.000
63-01	CLCFT	1816-00-1008	6.000
00C (SOT-23)	SIEM	4902-00-0809	9.000
79C-SOT-23	SIEM	4902-00-0170	6.000
-8GCJ101D	PNSNC	4711-05-1000	11.000
-8GCJ102D	PNSNC	4711-05-1001	3.000
-8GCJ222D	PNSNC	4711-05-2201	8.000
-8GCJ822D	PNSNC	4711-05-8201	2.000
-8GCJ160D	PNSNC	4711-05-1609	2.000
-8GCJ201D	PNSNC	4711-05-2000	4.000
-8GCJ151D	PNSNC	4711-05-1500	10.000
-8GCJ472D	PNSNC	4711-05-4701	3.000
-8GCJ331D	PNSNC	4711-05-3300	1.000
-8GCJ510D	PNSNC	4711-05-5109	10.000
-8GCJ100D	PNSNC	4711-05-1009	7.000

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
R622 R663 R665 R768	RES,CH,1/8W,5%,6.8K	RMC 1806825C	KMYO	4711-05-6801	4.000
R623 R637 R664 R666 R764	RES,CH,1/8W,5%,10000	ERJ-8GCJ103D	PNSNC	4711-05-1002	5.000
R624 R701 R710 R712 R722 R724 R725 R771 R779 R780	RES,CH,1/8W,5%,240	ERJ-8GCJ241D	PNSNC	4711-05-2400	10.000
R625 R636	RES,CH,1/8W,5%,1201	ERJ-8GCJ122D	PNSNC	4711-05-1201	2.000
R627 R638 R640 R655 R657 R700 R702	RES,CH,1/8W,5%,470	ERJ-8GCJ471D	PNSNC	4711-05-4700	7.000
R629 R631	RES,CH,1/8W,5%,390	ERJ-8GCJ391D	PNSNC	4711-05-3900	2.000
R630 R653	RES,CH,1/8W,5%,47	ERJ-8GCJ470D	PNSNC	4711-05-4709	2.000
R632	RES,CH,1/8W,5%,300	ERJ-8GCJ301D	PNSNC	4711-05-3000	1.000
R633 R635	RES,CH,1/8W,5%,15	ERJ-8GCJ150D	PNSNC	4711-05-1509	2.000
R634	RES,CH,1/8W,5%,56	ERJ-8GCJ560D	PNSNC	4711-05-5609	1.000
R641	RES,CH,1/8W,5%,820	ERJ-8GCJ821D	PNSNC	4711-05-8200	1.000
R645 R647	RES,CH,1/8W,5%,68	ERJ-8GCJ680D	PNSNC	4711-05-6809	2.000
R646	RES,CH,1/8W,5%,120	ERJ-8GCJ121D	PNSNC	4711-05-1200	1.000
R652 R654 R720 R721 R726 R727 R735 R736 R743 R744 R745 R746 R747 R748	RES,CH,1/8W,5%,24	ERJ-8GCJ240D	PNSNC	4711-05-2409	14.000
R658	RES,CH,1/8W,5%,12	ERJ-8GCJ120D	PNSNC	4711-05-1209	1.000
R662	RES,CH,1/8W,5%,270	ERJ-8GCJ271D	PNSNC	4711-05-2700	1.000
R704 R715	RES,CH,1/8W,5%,220	ERJ-8GCJ221D	PNSNC	4711-05-2200	2.000
R705 R716	RES,CH,1/8W,5%,36K	ERJ-8GC-363D	PNSNC	4711-05-3602	2.000
R708 R709	RES,CH,1/8W,5%,20	ERJ-8GCJ200D	PNSNC	4711-05-2009	2.000
R723 R659 R765 R769 R772	RES,CH,1/8W,5%,22K	RMC 1802235C	KMYO	4711-05-2202	5.000
R730	RES,CH,1/8W,1%,6.19K	RMC 1861971C	KMYO	4711-03-6191	1.000
R731 R760	RES,CH,1/8W,1%,12.1K	RMC1/8-12.1K	KMYO	4711-03-1212	2.000
R739	RES,CH,1/8W,1% 3.01K	RMC 1830111C	KMYO	4711-03-3011	1.000
R740	RES,CH,1/8,1%,14.7K	RMC 1814721C	KMYO	4711-03-1472	1.000
R749 R750	RES,CH,1/8W,5%,91	ERJ-8GCJ910D	PNSNC	4711-05-9109	2.000
R751	RES,C,1/8W,5%,36	ERJ-8GCJ360D	PNSNC	4711-05-3609	1.000
R752 R761	RES,CH,1/8W,1%,10.0K	RMC 1810021C	KMYO	4711-03-1002	2.000
R753 R754 R756 R759	RES,CH,1/8W,5%,330K	RMC 1803345C	KMYO	4711-05-3303	4.000
R755	RES,CH,1/8W,5%,39K	RMC 1803935C	KMYO	4711-05-3902	1.000
R758	RES,CH,1/8W,5%,30K	RMC 1803035C	KMYO	4711-05-3002	1.000

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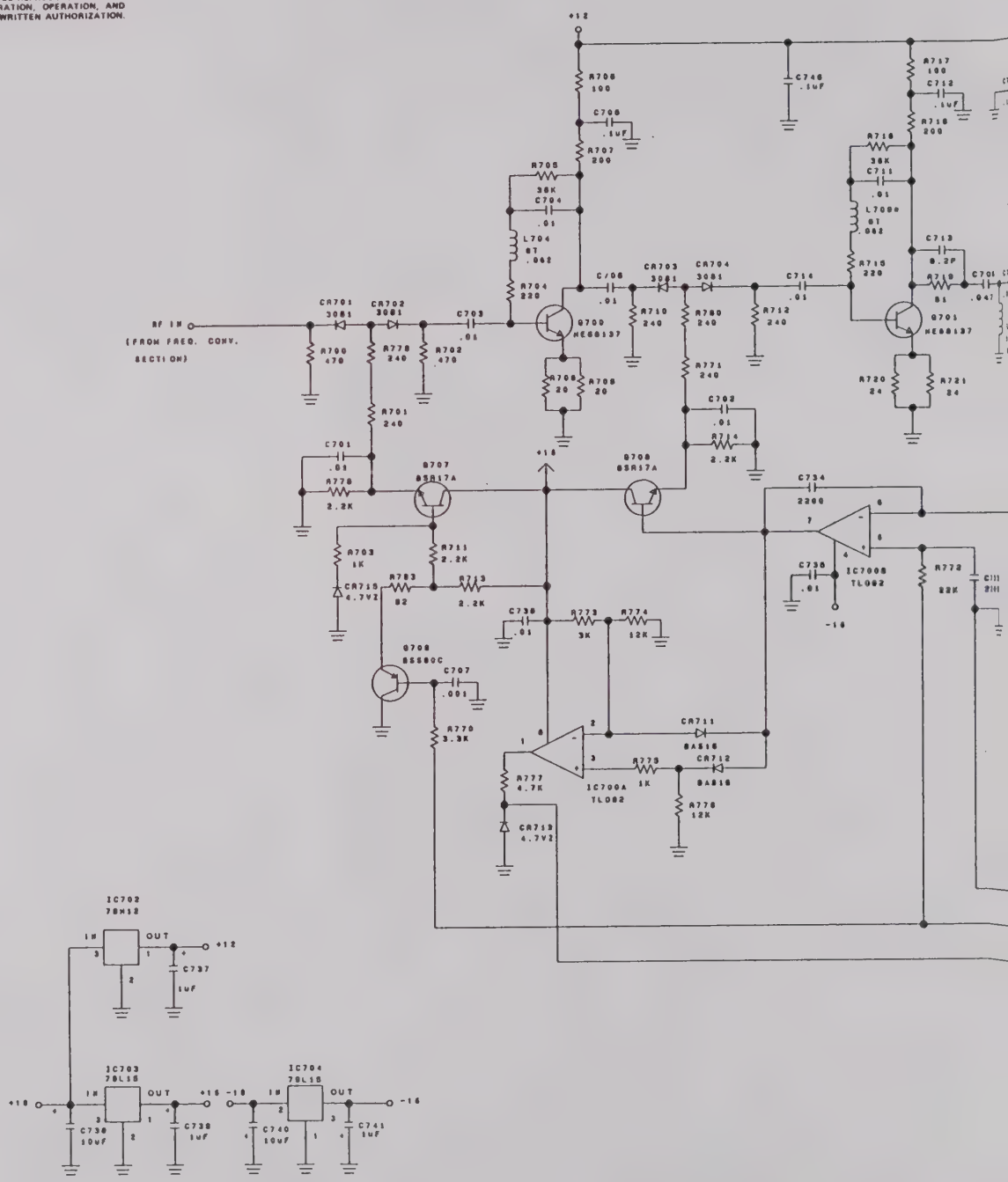

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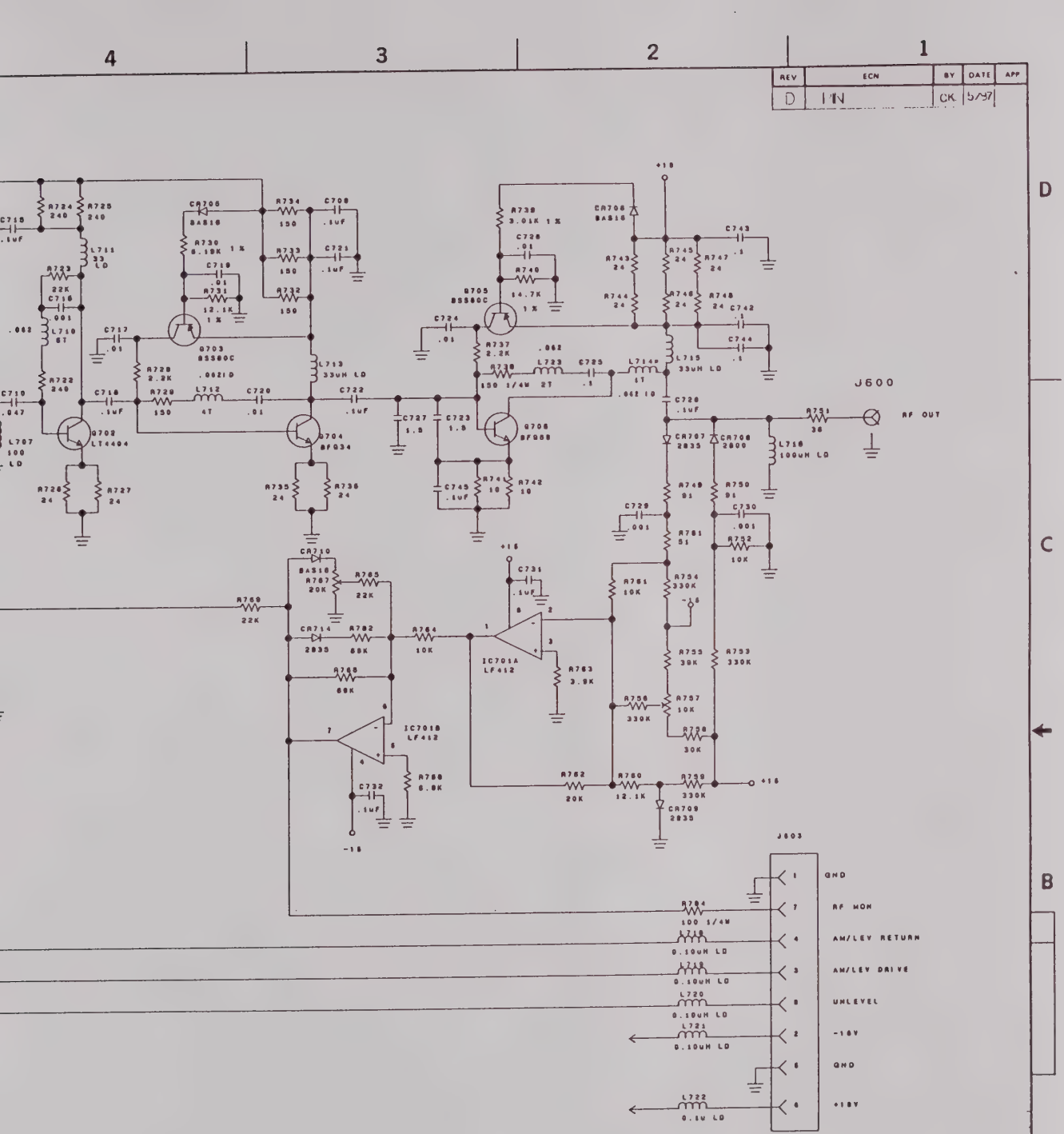

FIGURE 10-12

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN C. KEISER	DATE 5/67	WAVETEK
MATERIAL	PROJENGR		TITLE AMP BOARD LEVELER SECTION
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG		MODEL NO 2500 / DWG NO 0014-30-0363 / REV D
	SCALE		CODE (DEPT) 34280 / SHEET 2 OF 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
R762	RES,CH,1/8W,5%,20K	ERJ-8GC-203D	PNSNC	4711-05-2002	1.000
R763	RES,CH,1/8W,5%,3.9K	RMC 1803925C	KMYO	4711-05-3901	1.000
R766 R782	RES,CH,1/8W,5%,68K	RMC 1806835C	KMYO	4711-05-6802	2.000
R770	RES,CH,1/8W,5%,3300	ERJ-8GCJ332D	PNSNC	4711-05-3301	1.000
R773	RES,CH,1/8W,5%,3000	ERJ-8GCJ302D	PNSNC	4711-05-3001	1.000
R774 R776	RES,CHIP,1/8W,5%,12K	ERJ-8GCJ-123D	PNSNC	4711-05-1202	2.000
R783	RES,CH,1/8W,5%,82	ERJ-8GCJ820D	PNSNC	4711-05-8209	1.000

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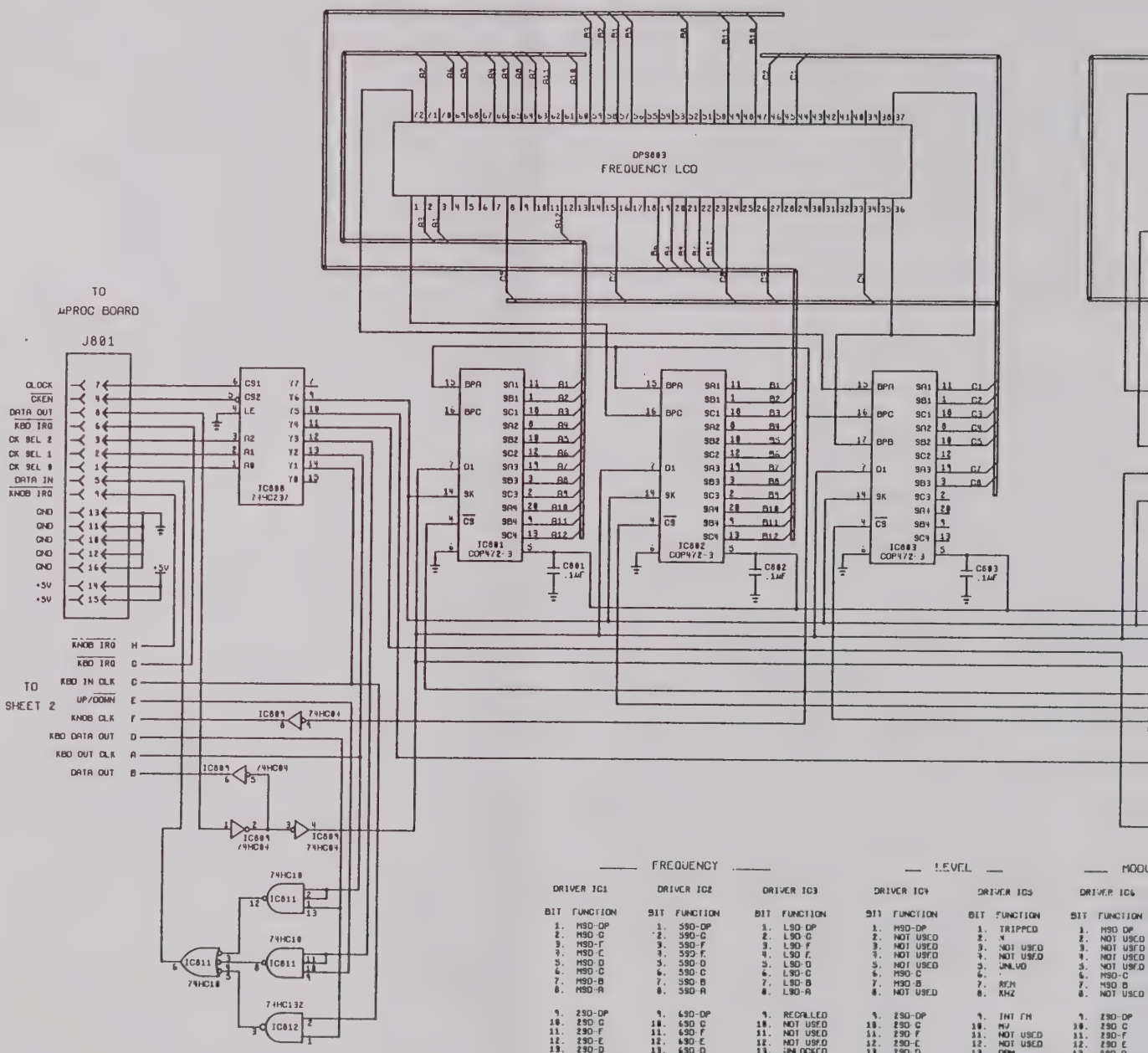

	FREQUENCY			LEVEL		MODU
DRIVER IC1	DRIVER IC2	DRIVER IC3	DRIVER IC4	DRIVER IC5	DRIVER IC6	
BIT FUNCTION	BIT FUNCTION	BIT FUNCTION	BIT FUNCTION	BIT FUNCTION	BIT FUNCTION	
1. MSD-DP	1. 590-DP	1. LSD-DP	1. MSD-DP	1. TRIPPED	1. MSD DP	
2. MSD-G	2. 590-G	2. LSD-G	2. NOT USED	2. %	2. NOT USED	
3. MSD-F	3. 590-F	3. LSD-F	3. NOT USED	3. NOT USED	3. NOT USED	
4. MSD-E	4. 590-E	4. LSD-E	4. NOT USED	4. NOT USED	4. NOT USED	
5. MSD-D	5. 590-D	5. LSD-D	5. NOT USED	5. UNLVD	5. NOT USED	
6. MSD-C	6. 590-C	6. LSD-C	6. MSD-C	6. -	6. MSD-C	
7. MSD-B	7. 590-B	7. LSD-B	7. MSD-B	7. RCM	7. MSD B	
8. MSD-A	8. 590-A	8. LSD-A	8. NOT USED	8. KHZ	8. NOT USED	
9. 2SD-DP	9. 690-DP	9. RECALLED	9. 2SD-DP	9. INT FM	9. 2SD-DP	
10. 2SD-G	10. 690 G	10. NOT USED	10. 2SD G	10. MV	10. 2SD G	
11. 2SD-F	11. 690-F	11. NOT USED	11. 2SD F	11. NOT USED	11. 2SD-F	
12. 2SD-E	12. 690-E	12. NOT USED	12. 2SD-E	12. NOT USED	12. 2SD E	
13. 2SD-D	13. 690 D	13. UNLOCKED	13. 2SD D	13. OBM	13. 2SD D	
14. 2SD-C	14. 690-C	14. MHZ	14. 2SD C	14. NOT USED	14. 2SD-C	
15. 2SD-B	15. 690-B	15. STORED	15. 2SD B	15. INT AM	15. 2SD B	
16. 2SD-A	16. 690-A	16. NOT USED	16. 2SD A	16. MV	16. 2SD A	
17. 3SD-DP	17. 790-DP	17. EXT REF	17. 3SD-DP	17. RF OFF	17. 3SD DP	
18. 3SD-G	18. 790-G	18. NOT USED	18. 3SD-G	18. NOT USED	18. 3SD G	
19. 3SD-F	19. 790-F	19. NOT USED	19. 3SD-F	19. V	19. 3SD F	
20. 3SD-E	20. 790 E	20. NOT USED	20. 3SD E	20. NOT USED	20. 3SD-E	
21. 3SD-D	21. 790-D	21. CAL	21. 3SD D	21. 1000HZ	21. 3SD D	
22. 3SD-C	22. 790-C	22. NOT USED	22. 3SD C	22. NOT USED	22. 3SD C	
23. 3SD-B	23. 790-B	23. NOT USED	23. 3SD-B	23. RF ON	23. 3SD B	
24. 3SD-A	24. 790-A	24. NOT USED	24. 3SD-A	24. 400 HZ	24. 3SD-A	
25. 4SD-DP	25. 890-DP	25. NOT USED	25. 4SD-DP	25. EXT FM	25. 4SD-DP	
26. 4SD-G	26. 890-G	26. NOT USED	26. 4SD-G	26. NOT USED	26. 4SD G	
27. 4SD-F	27. 890-F	27. NOT USED	27. 4SD-F	27. NOT USED	27. 4SD-F	
28. 4SD-E	28. 890-E	28. NOT USED	28. 4SD-E	28. NOT USED	28. 4SD-E	
29. 4SD-D	29. 890-D	29. NOT USED	29. 4SD-D	29. NOT USED	29. 4SD-D	
30. 4SD-C	30. 890-C	30. NOT USED	30. 4SD-C	30. NOT USED	30. 4SD-C	
31. 4SD-B	31. 890-B	31. NOT USED	31. 4SD-B	31. EXT AM	31. 4SD-B	
32. 4SD-A	32. 890-A	32. NOT USED	32. 4SD-A	32. NOT USED	32. 4SD-A	
33. MSB-CURSOR	33. 5SB-CURSOR	33. 1SB-CURSOR	33. NOT USED	33. NOT USED	33. NOT USED	
34. 2SD-CURSOR	34. 6SD-CURSOR	34. NOT USED	34. 2SD-CURSOR	34. NOT USED	34. 2SD-CURSO	
35. 3SD-CURSOR	35. 7SD-CURSOR	35. NOT USED	35. 3SD-CURSOR	35. NOT USED	35. 3SD-CURSO	
36. 4SD-CURSOR	36. 8SD-CURSOR	36. NOT USED	36. 4SD-CURSOR	36. NOT USED	36. 4SD-CURSO	
37. NOT USED	37. NOT USED	37. NOT USED	37. NOT USED	37. NOT USED	37. NOT USED	
38. Q6	38. Q6	38. Q6	38. Q6	38. Q6	38. Q6	
39. Q7	39. Q7	39. Q7	39. Q7	39. Q7	39. Q7	
40. STND	40. STND	40. STND	40. STND	40. STND.	40. STND	

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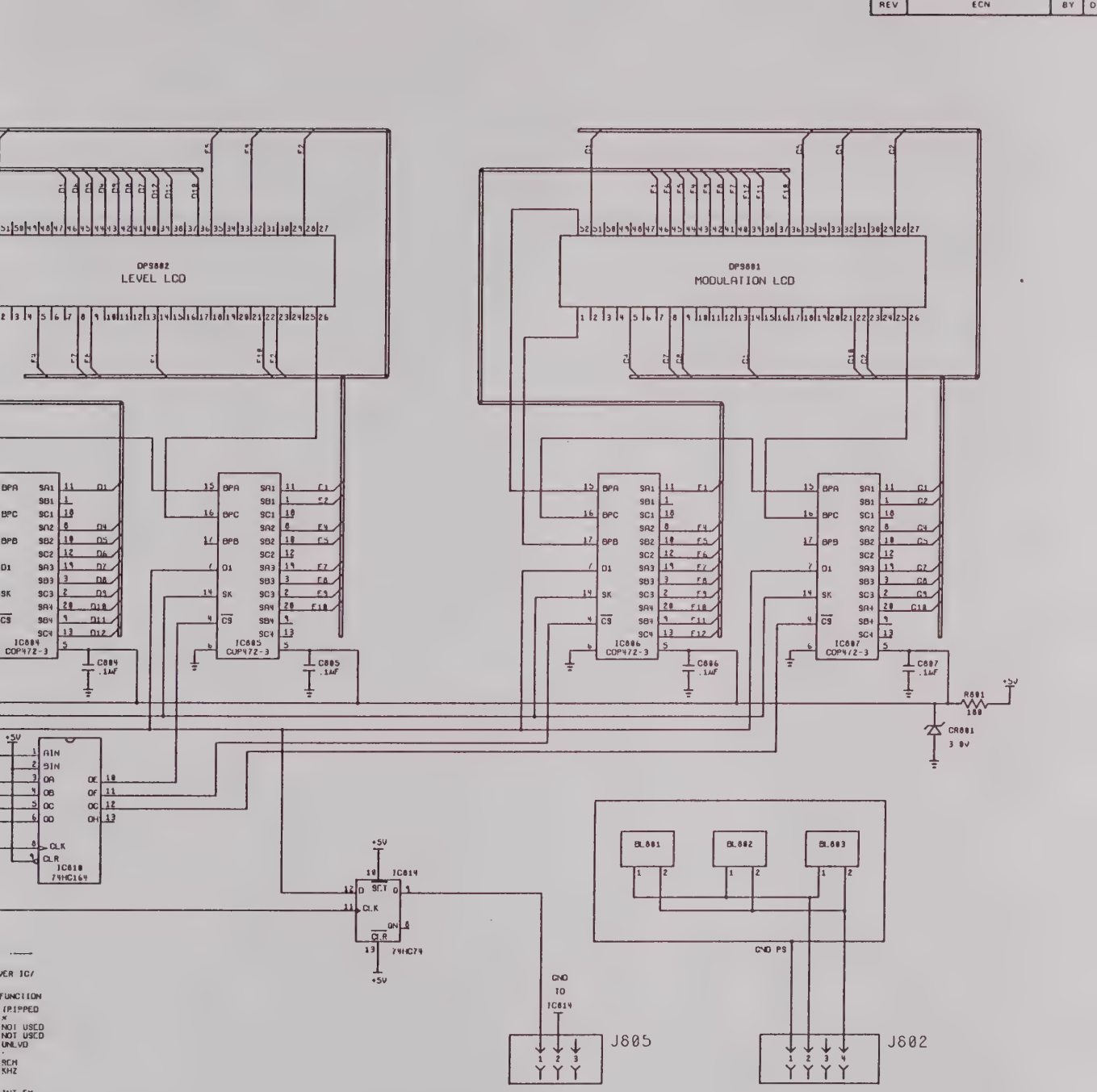

FIGURE 10-13

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. ABEL	DATE 09:23	WAVETEK
MATERIAL	PROJ ENGR T. STUCKER	16 MAR 1987	TITLE MFG / ENGR CHECK SET
	RELEASE APPROV T. DUDZIAK		SCHEMATIC DISPLAY BD
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG	MODEL NO 2500	DWG NO. 0014-30-0351
	SCALE N/A	CODE IDENT 34280	C11A SHEET 6
	M 85022.RB /V59 FAB		

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
1	LO SHIELD FOR OSC BD PER B/P	1410-30-7860	W-I	1410-30-7860	1.000
2	DOUBLER SHIELD FOR OSC BD, PER B/P	1410-30-7870	W-I	1410-30-7870	1.000
3	LEVELER SHIELD FOR OSC BD,PER B/P	1410-30-7880	W-I	1410-30-7880	1.000
C658 C682 C737 C739 C741	CAP,TANT,25V,1UF	100DE105K25A2	ACI	1510-21-7010	5.000
C683 C738 C740	CAP,TANT,25V,10UF	100DE106M20C2	ACI	1510-21-7100	3.000
CR624 CR713 CR715	DIODE,ZENER,1W,GP DO-41,V=4.7,IT=53mA IF=193mA,+/-10%,SS#2	1N4732	MOT	4801-01-4732	3.000
CR701 CR702 CR703 CR704	DIODE,PIN,GP SWIT AXIAL,V=100V CT=0.4pF,SS#2	5082-3081	H-P	4805-02-0004	4.000
CR707 CR709 CR714	DIODE,SCHOTTKY,LOW OFFSET AXIAL,V=5V CT=1.6pF,SS#1	5082-2835	H-P	4809-02-0002	3.000
CR708	DIODE,HOT CARR,GP AXIAL,V=70V IR=200nA IR=100nA,CT=1pF,SS#1	5082-2800	H-P	4809-02-0001	1.000
G600	FREQ DOUBLER	SK-2	MIN-C	3010-51-0002	1.000
IC600 IC603	VOLT REG,+5V STATIC SENSITIVE #2	MA78L05AWC	FCD	7000-78-0501	2.000
IC601	HEX BUS DRIVER STATIC SENSITIVE	SN74LS368AN	T-I	8007-43-6810	1.000
IC602	HI SPEED D FLIP-FLOP STATIC SENSITIVE	11C06	FCD	8000-11-0600	1.000
IC700	DUAL OP AMP STATIC SENSITIVE #2	TL082CP	T-I	7000-00-8200	1.000
IC701	DUAL JFET INPUT OPERATIONAL AMP STATIC SENSITIVE #2	LF412CN	NAT	7000-04-1210	1.000
IC702	POS VOLT REG,12 V STATIC SENSITIVE #2	UA78M12UC	FCD	7000-78-1200	1.000
IC703	VOLT REG, +15 STATIC SENSITIVE #2	MC78L15CP	MOT	7000-78-1510	1.000
IC704	VOLT,REG,FIXED,-15V PLAS,TO-226AA,-33Vdc 10%,Io=100mA,SS#2	MC79L15CP	MOT	7000-79-1510	1.000
J603A J603B	MOD RECEPT,PC MT,.1" CTR,10 PIN,TOP ENTRY FROM:2112-35-0010	2112-35-0012	W-I	2112-35-0012	2.000
KIT	HYBRID PT KT,AMP BD, 2500	2500-AMP-HYBRID-KT	W-I	1219-00-0630	1.000

REFERENCE DESIGNATORS	PART DESCRIPTION
L602	COIL,AIR,4T,28GA, .100 ID
L608 L610 L612 L628 L630 L632	COIL,AIR,4T,28GA, .100 ID
L609 L615 L644 L645	COIL,AIR,4T,28 GA, .062 ID
L611 L617 L629 L633	COIL,AIR,5T,28 GA, .100 ID
L613 L631	COIL,AIR,6T,28 GA .100 ID
L614 L653	COIL,AIR,3T,28GA, .100 ID
L618 L619 L621 L623 L624 L646 L649 L650 L652 L655 L717 L718 L719 L720 L721 L722	CHOKE,COATED,0.10UH 10%,D=0.120 IN, L=0.300IN,I=1350MA
L625 L707 L716	CHOKE,COATED,100UH 10%,D=0.120IN, L=0.300IN,I=84MA
L641	COIL,AIR,2T,28GA, .100 ID
L647 L648	COIL,AIR,7T,28 GA .100 ID
L704 L709# L710	COIL,AIR,28GA,6T, .062 ID
L711 L713 L715	CHOKE,COATED,33UH 10%,D=0.120IN L=0.300,I=130MA
L712	COIL,AIR,4T,28GS, .062 ID
L714# L723	COIL,AIR,2T,28 GA .062 ID
MX600	MIXER,DBL.BAL.
Q601 Q606	NPN,317-0112,H Freq F=3G,V=18,Ices=1mA P=2W,hFE=200,SS#2
Q608 Q700 Q701	NPN,TO-37,AMP F=9G,V=10,JCBO=1.0uA P=250mW,HFE=100,SS#2
Q702	NPN,SMD,IF AMP F=5G,VCBO=30,Icbo=1u I=70mA,hFE=50,SS#2
Q704	XSTOR, LINEAR POWER STATIC SENSITIVE #2

WAVETEK PARTS LIST | AMPLIFIER BD,2500

RIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
015-00-0184	W-I	1815-00-0184	1.000
015-00-0185	W-I	1815-00-0185	6.000
015-00-0173	W-I	1815-00-0173	4.000
015-00-0175	W-I	1815-00-0175	4.000
015-00-0176	W-I	1815-00-0176	2.000
815-00-0182	W-I	1815-00-0182	2.000
0HR10	JEF	1810-03-0019	16.000
0N101	JEF	1810-03-0101	3.000
815-00-0181	W-I	1815-00-0181	1.000
815-00-0177	W-I	1815-00-0177	2.000
815-00-0180	W-I	1815-00-0180	3.000
0N330	JEF	1810-03-0330	3.000
815-00-0183	W-I	1815-00-0183	1.000
815-00-0178	W-I	1815-00-0178	2.000
L-1-DBL	MIN-C	3010-54-0004	1.000
F559	MOT	4902-00-5590	2.000
E60137	NEC	4902-60-1370	3.000
T4404	TRW	4902-04-4040	1.000
T034	APX	4902-00-0341	1.000

	1218-00-2300	E
	PAGE: 2	REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
Q706	XSTOR STATIC SENSITIVE #2	BF068	APX	4902-00-0680	1.000
R668	RES,C,1/4W,5%,300	CF1/4-300	ASE	4700-15-3000	1.000
R675	RES,C,1/4W,5%,51	CF1/451	ASE	4700-15-5109	1.000
R676	RES,C,1/4W,5%,820	CF1/4-820	ASE	4700-15-8200	1.000
R738	RES,C,1/4W,5%,150	CF1/4-150	ASE	4700-15-1500	1.000
R757	TRM,CM,L,10K,10%,PC 11,PN,CW,.19H,.375W .375L,TA	3386R-1-103	BOU	4610-00-3103	1.000
R767	TRM,CM,L,20K,10%,PC 11,PN,CW,.19H,.375W .375L,TA	3386R-1-203	BOU	4610-00-3203	1.000
R784	RES,C,1/4W,5%,100	CF1/4-100	ASE	4700-15-1000	1.000
SCH	SCH,AMP BD,2500	0014-30-0363	W-I	0014-30-0363	1.000

WAVETEK PARTS LIST	AMPLIFIER BD,2500	1218-00-2300 PAGE: 3	E REV

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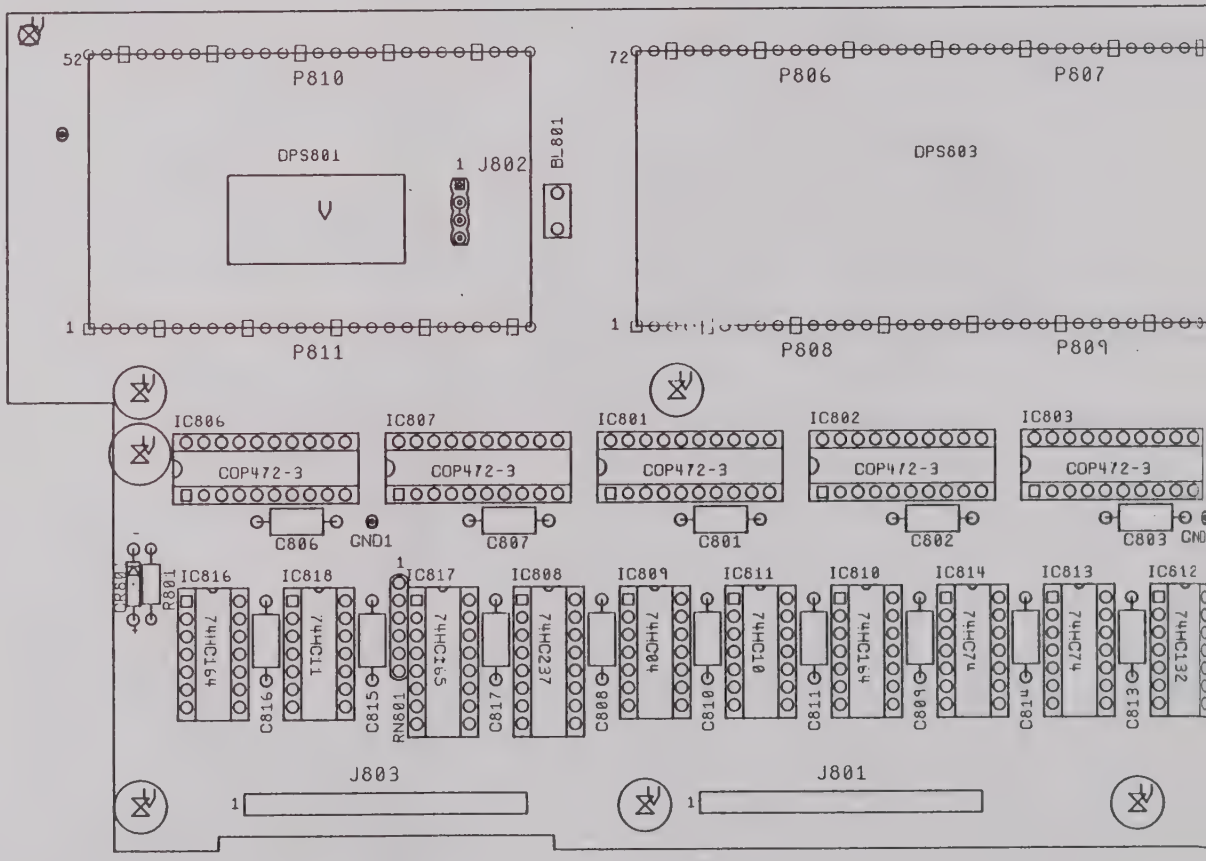

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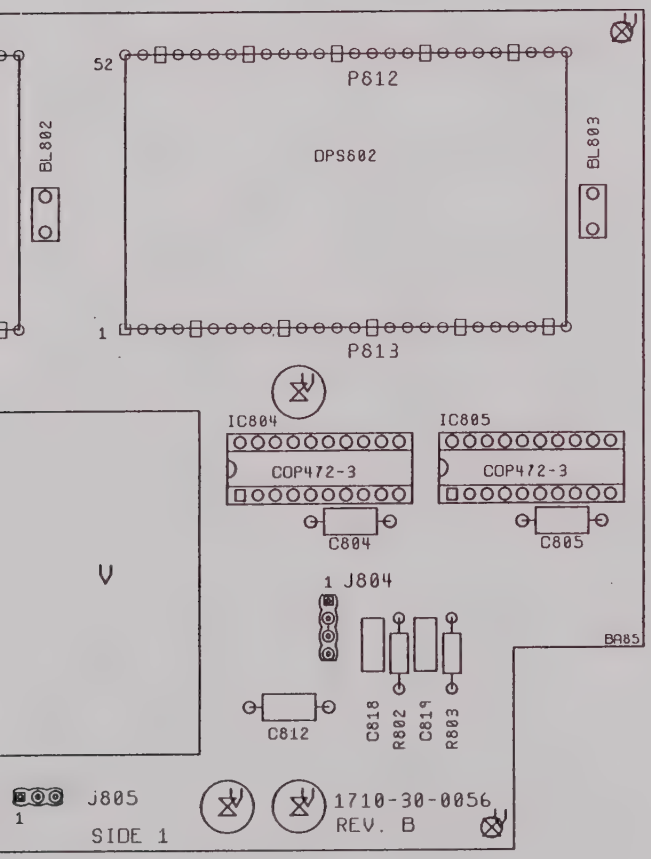

FIGURE 10-13A

REV	ECN	BY	DA

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK
MATERIAL	PROJENGR T. STUCKER	16 MAR	TITLE MFG / ENGR CHECK SET
	RELEASE APPROV T. DUDZIAK		TOP ASSEMBLY DW
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ANGLES .XX		DISPLAY BD
	DO NOT SCALE DWG	MODEL NO 2500	DWG NO 0012-30-0017
	SCALE 2:1	CODE IDENT 34260	SHEET 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
BL801 BL803	BACK-LIGHT PACKAGE LIT AREA 0.80X2.65	221-21112	MICRL	2410-02-0015	2.000
BL802	BACK-LIGHT PACKAGE, LIT AREA 0.80X3.60	223-21112	MICRL	2410-02-0014	1.000
C801 C802 C803 C804 C805 C806 C807 C808 C809 C810 C811 C812 C813 C814 C815 C816 C817	.1 MF 20%,50V,GENERL PURPOSE AXIAL LEAD TAPE AND REEL	SA205E1042AA	AVX	1510-17-1104	17.000
C818 C819	.01 MF 10%,50V STABL AXIAL LEAD CAP TAPE AND REEL	C410C103K5R5CA	KEMET	1510-17-1103	2.000
CR801	DIODE,ZENER,0.5W,GP AXIAL,V=3V4/-5%,SS#2	1N4372	MOT	4801-01-4372	1.000
DPS801 DPS802	LCD DISPLAY-CUSTOM MODLATION/LEVEL	2410-03-0015PER DESC	HMLN	2410-03-0015	2.000
DPS803	LCD DISPLAY-CUSTOM FREQUENCY	2410-03-0014PER DESC	HMLN	2410-03-0014	1.000
GND01 GND02	HEADER,1-PIN,STRT REF:2112-07-0000	65501-401	BER	2112-07-0020	2.000
IC801 IC802 IC803 IC804 IC805 IC806 IC807	LCD DISPLAY,CONTROLR PLAS,DIP-20,5Vdc CMOS,SS#2	CDP472N-3	NAT	8000-47-2310	7.000
IC808	1 OF 8 DECODER/DEMUX STATIC SENSITIVE	MC74HC237N	MOT	8007-42-3710	1.000
IC809	HEX INVERTER, STATIC SENSITIVE	MC74HC04N	MOT	8000-74-0411	1.000
IC810 IC816	8-BIT SER INPUT/PARA OUTPUT SHIFT REGISTR STATIC SENSITIVE	SN74HC164N	T-I	8007-41-6411	2.000
IC811	3-INPUT NAND GATE STATIC SENSITIVE	MC74HC10	MOT	8000-74-1001	1.000
IC812	QUAD 2-INPUT NAND SCHMITT TRIGGER STATIC SENSITIVE	MM74HC132N	NAT	8007-41-3211	1.000
IC813 IC814	2-D TYP,POS EDG TRIG FLIP-FLOP W/CLR&PRE-SET,STATIC SENSITIVE	MC74HC74	MOT	8000-74-7403	2.000
IC817	8-BIT SER OR PAR-IN/ SER-OUTPUT SHIFT REG STATIC SENSITIVE	SN74HC165N	T-I	8007-41-6510	1.000
IC818	TRIPLE 3-INPUT AND GATE STATIC SENSITIVE	SN74HC11N	T-I	8000-74-1111	1.000
J802 J804	HEADER,4-PIN,R.A. REF:2112-08-0000	65524-404	BER	2112-08-0004	2.000

REFERENCE DESIGNATORS	PART DESCRIPTION
J805	HDR,RA,3-PIN REF:2112-08-0000
P806 P807 P808 P809	SOCKET,18 SIL PER B/P 0019-00-0026 FROM:2412-00-0080
P810 P811 P812 P813	SCOCKET,26 SIL
R801	RES,C,1/4W,5%,180
R802 R803	RES,C,1/4W,5%,47K
RN801	RES,NW,10K,SIP,2% 3/4W,BUSSED, 5 RES TC=100PPM
SCH	SCH, DISPLAY BD,2500
W14	FLAT CABLE,5.5 IN, 16-CONDUCTORS

MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
-403	BER	2112-08-0018	1.000
00-0080	W-I	2112-00-0080	4.000
00-10	ARIES	2112-00-0078	4.000
-180	ASE	4700-15-1800	1.000
-47K	ASE	4700-15-4702	2.000
1-R10K	CTSBR	4770-00-0002	1.000
30-0351	W-I	0014-30-0351	1.000
.5E-E	T-B	6011-60-0073	1.000

	1218-00-2280 PAGE: 2	B REV

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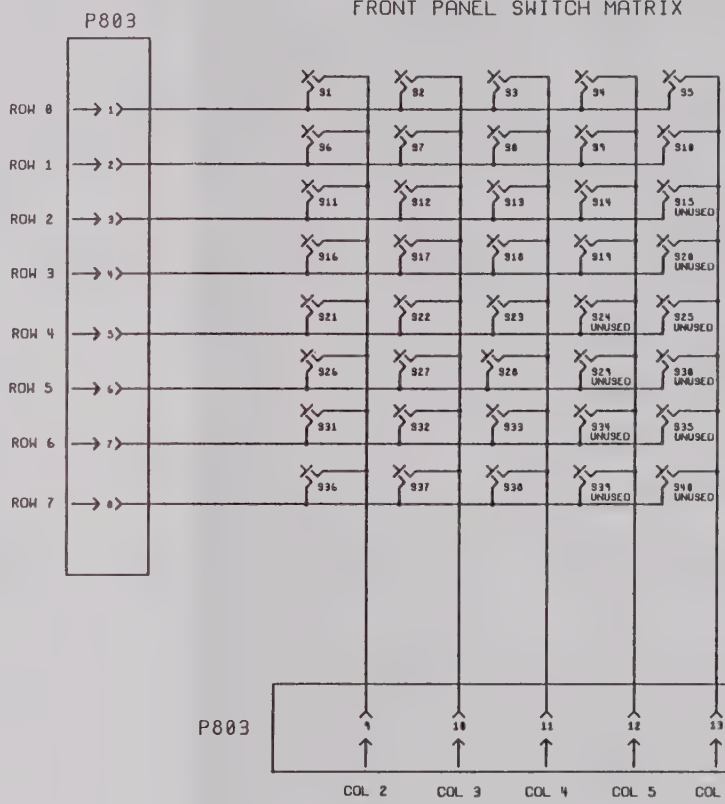
FRONT PANEL SWITCH MATRIX



SWITCH MATRIX DECODING

DEFINED

ROW 7	ROW 6	ROW 5	ROW 4	ROW 3	ROW 2	ROW 1	ROW 0
1	1	1	1	1	1	1	0

APPLYING A
ACTIVITY I
TO BE DETE

COL 7	COL 6	COL 5	COL 4	COL 3	COL 2	COL 1	COL 0
0	1	1	1	1	0	0	0

THE COLUMN
OF THE SWI
BEING DEPR
VALUE OF 7
FOR ROW EX

SET EQUAL
RESERVED F

USED FOR C

NOT USED F
TO EQUAL 0

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY

SWITCH MATRIX DECODING

SWITCH	ROW	COLUMN	KEY NAME
S1	FE	78	MHZ/MV
S2	FE	74	KHZ uV
S3	FE	6C	*/DBM
S4	FE	5C	RF ON/OFF
S5	FE	3C	RIGHT ARROW
S6	FD	78	9
S7	FD	74	6
S8	FD	6C	3
S9	FD	5C	+/-
S10	FD	3C	LEFT ARROW
S11	FB	78	8
S12	FB	74	5
S13	FB	6C	2
S14	FB	5C	.
S15	FB	3C	NOT USED
S16	F7	78	7
S17	F7	74	4
S18	F7	6C	1
S19	F7	5C	DEC. POINT
S20	F7	3C	NOT USED
S21	EF	78	FREQ
S22	EF	74	LVL
S23	EF	6C	INIT.
S24	EF	5C	NOT USED
S25	EF	3C	NOT USED
S26	DF	78	STR
S27	DF	74	RCL
S28	DF	6C	LCL
S29	DF	5C	NOT USED
S30	DF	3C	NOT USED
S31	BF	78	INT FM
S32	BF	74	EXT FM
S33	BF	6C	MOD OFF
S34	BF	5C	NOT USED
S35	BF	3C	NOT USED
S36	7F	78	INT AM
S37	7F	74	EXT AM
S38	7F	6C	400/1000
S39	7F	5C	NOT USED
S40	7F	3C	NOT USED

YTE OF FE ALLOWS
CHES S1 THRU S5
.

IS READ TO DETERMINE WHICH
IN THE ACTIVATED ROW IS

CATES THAT S1 IS ACTIVATED
OF FE.

N THIS APPLICATION
URE USE.

DECODING

UMN DECODING

FIGURE 10-15

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R ABEL	DATE 09:25 25SEP 1986	WAVETEK
MATERIAL	PROJENGR T STUCKER		TITLE MFG / ENGR CHECK SET
	RELEASE APPROV T DUDZIAK		SCHEMATIC KEYBOARD
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG	MODEL NO 2500	DWG NO 0014-30-035
	SCALE N/A	CODE IDENT 34280	CTM SHEET 6
	TM.85023.RB /V13.FAB		

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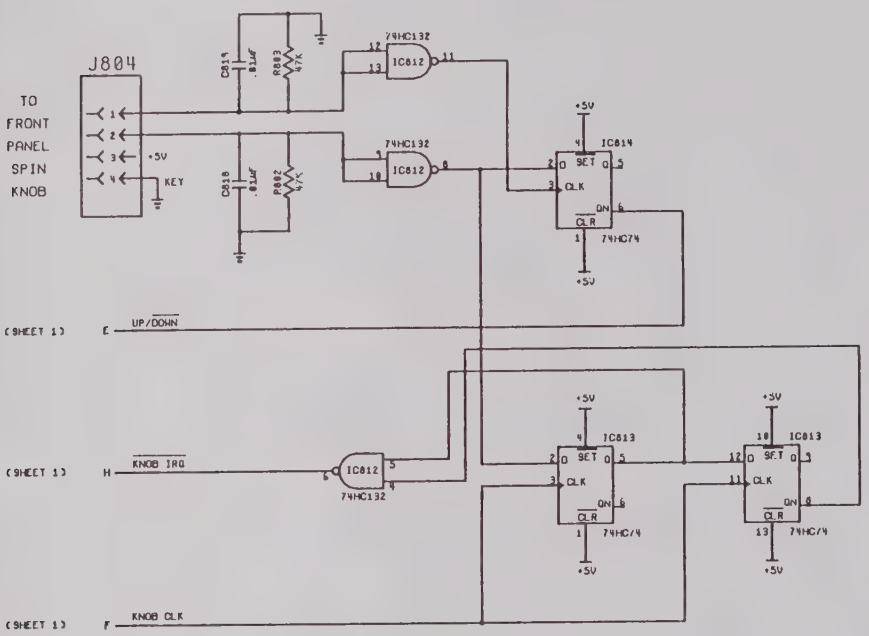

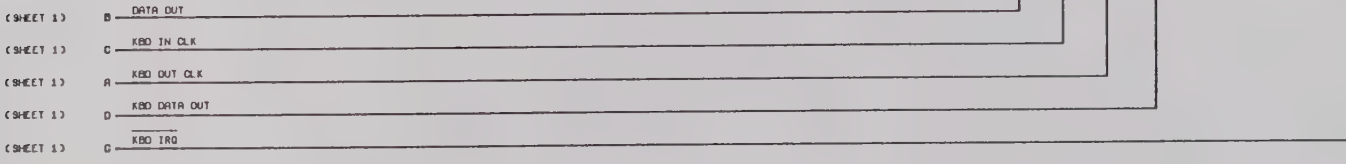

SHEET 6

ICN	DE
IC801-807	CO
IC808	74
IC809	74
IC811	74
IC814	74
IC818	74

NOTE UNLESS OTHERWISE SPECIFIED

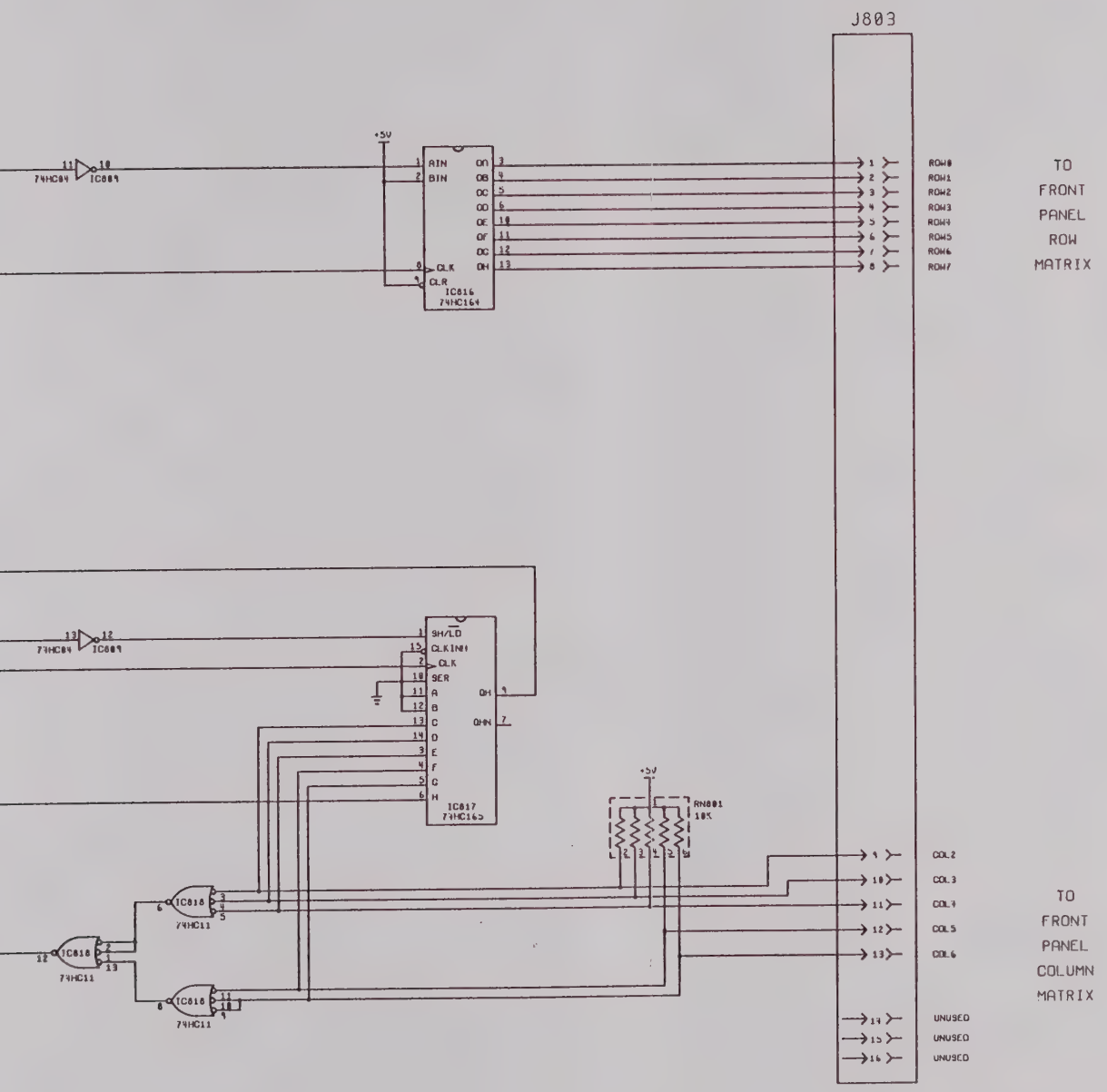

FIGURE 10-14

IC POWER & GROUND TABLE

SHEET 7

GND	+5V
6	5
8	16
7	14
7	14
7	14
7	14

ICN	DEVICE	GND	+5V
IC812	74HC132	7	14
IC813	74HC74	7	14
IC816	74HC164	7	14
IC817	74HC165	8	16
IC818	74HC11	7	14

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. ABEL	DATE 09:23 16MAR 1987	WAVETEK
MATERIAL	PROJ ENGR T. STUCKER		TITLE MFG / ENGR CHECK SET
	RELEASE APPROV T. DUDZIAK		SCHEMATIC DISPLAY BD
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG SCALE N/A	MODEL NO 2500	DWG NO 0014-30-0351 REV B
	M.65022.RB /V59.FAB	CODE IDENT 34280	C12A SHEET 7 OF 8

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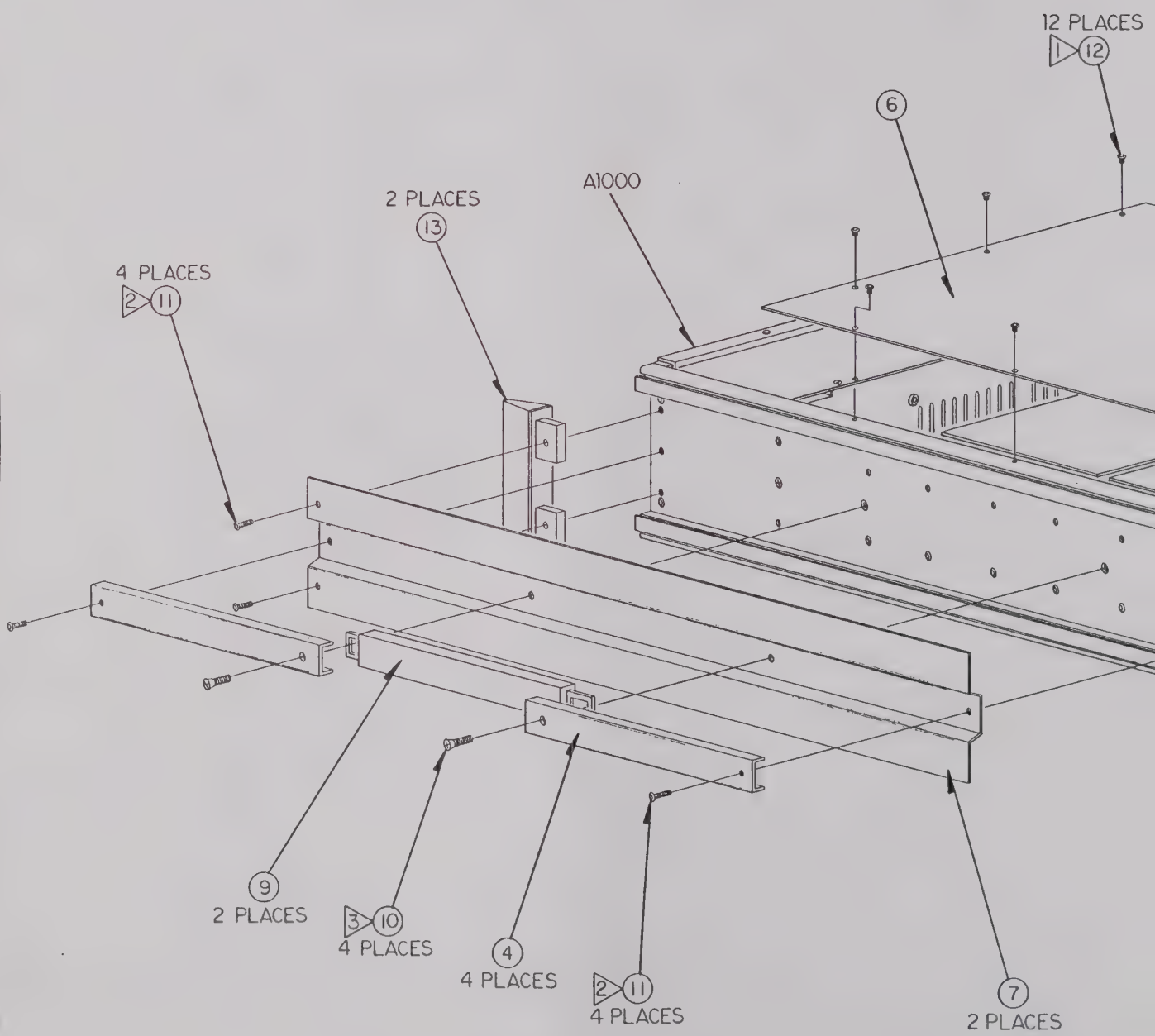
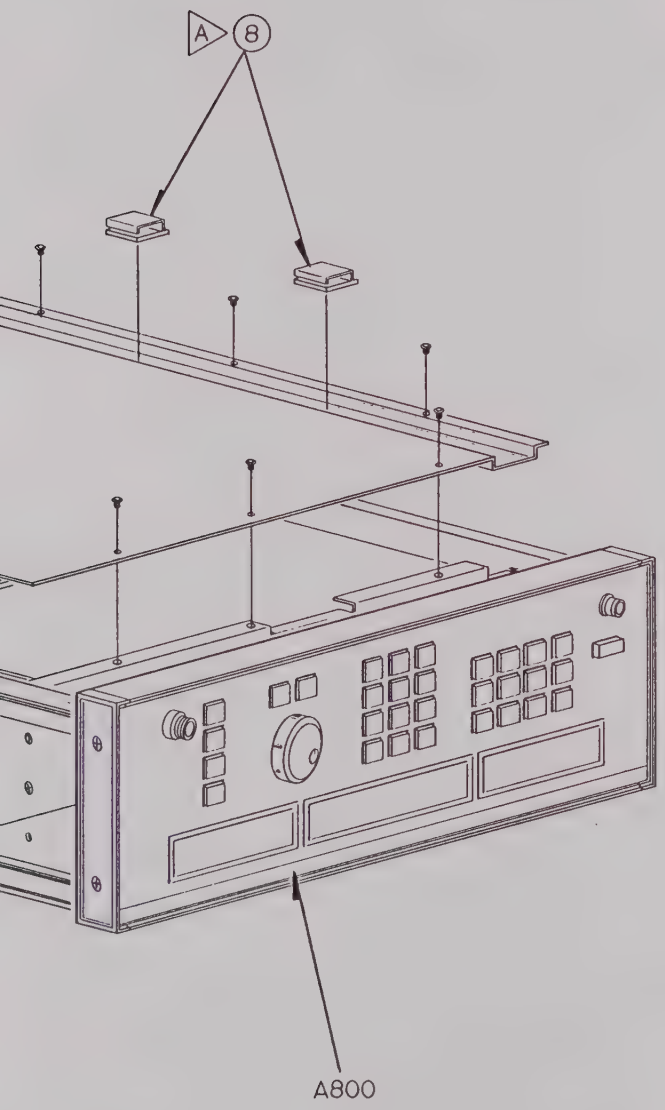


NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DA



(A) THERE IS A TOTAL OF 4 CABLE CLAMPS USED. ONE IS ATTACHED TO THE INSIDE OF EACH SIDE PANEL (THESE TWO ARE NOT SHOWN)

(1) TORQUE TO 4.7 IN-LBS

(2) TORQUE TO 8.7 IN-LBS

(3) TORQUE TO 29.7 IN-LBS

REFERENCE BOM *1111-00-0179

FIGURE 10-16A

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK
MATERIAL	PROJ ENG	2/6/	TITLE
	RELEASE APPROV	2/11/96	WRAP-UP KIT
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ANGLES .XX		DRAWING
	DO NOT SCALE DWG	MODEL NO. 2500	DWG NO. 0012-30-003
	SCALE 1/2	CODE IDENT 34280	SHEET 1

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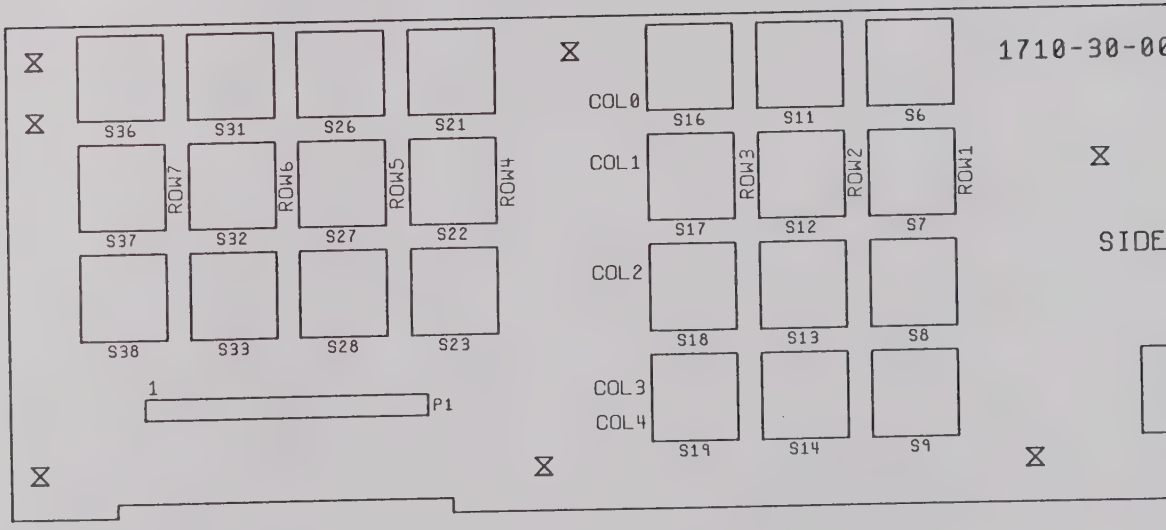

NOTE UNLESS OTHERWISE SPECIFIED

8 | 7 | 6 | 5

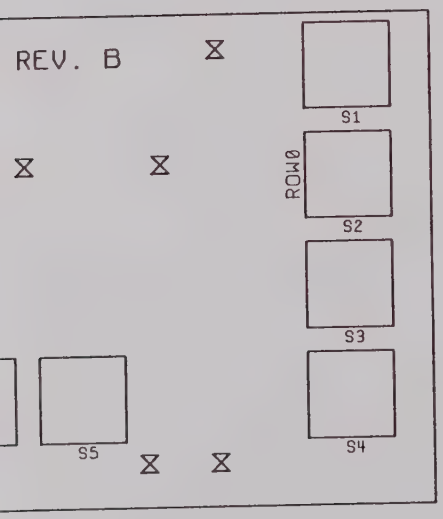

FIGURE 10-15A

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BOB ABEL	DATE 09:22	WAVETEK
MATERIAL	PROJENGR D. BADGER	25SEP 1986	TITLE MFG / ENGR CHECK SET
	RELEASE APPROV T. DUDZIAK		TOP ASSEMBLY DWG KEYBOARD
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG	MODEL NO 2500	DWG NO 0012-30-0019
	SCALE 2:1	CODE IDENT 34280	C2A SHEET 3 OF
	TM 85823.RB /V12.FAB		

4 3 2 1

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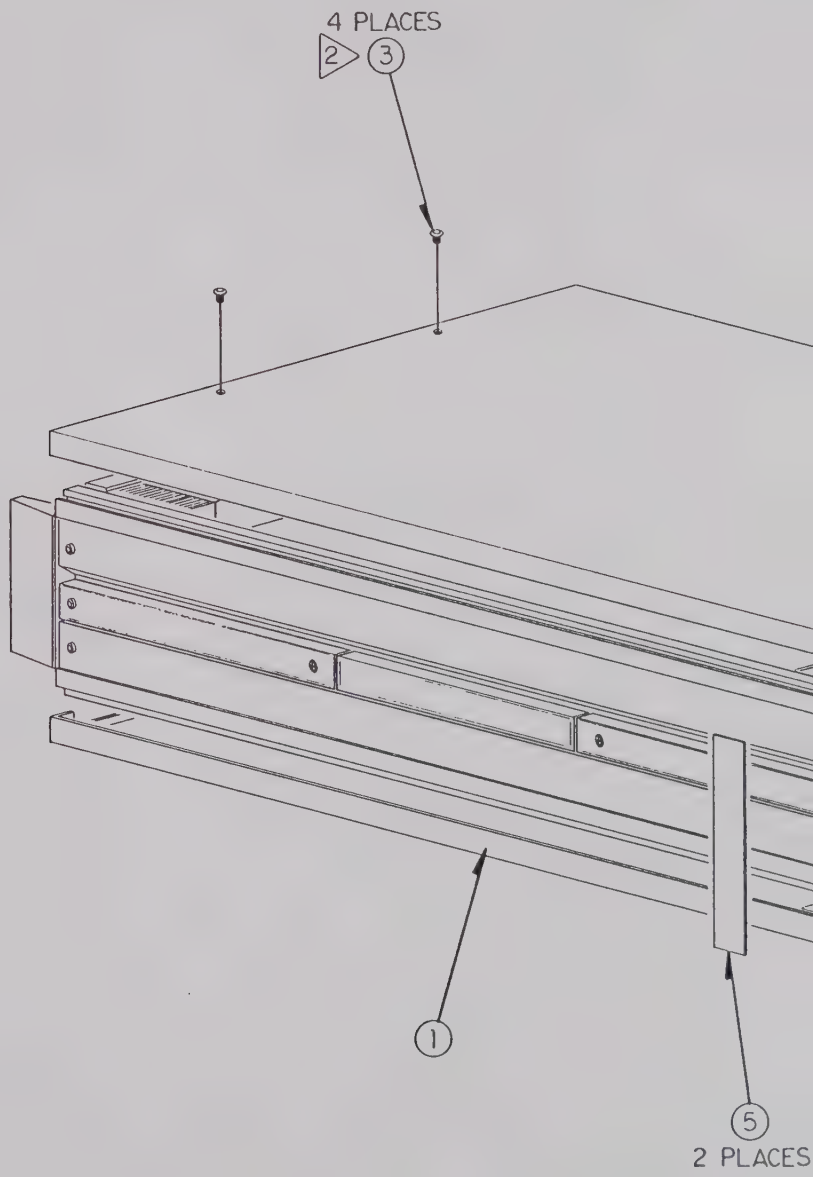
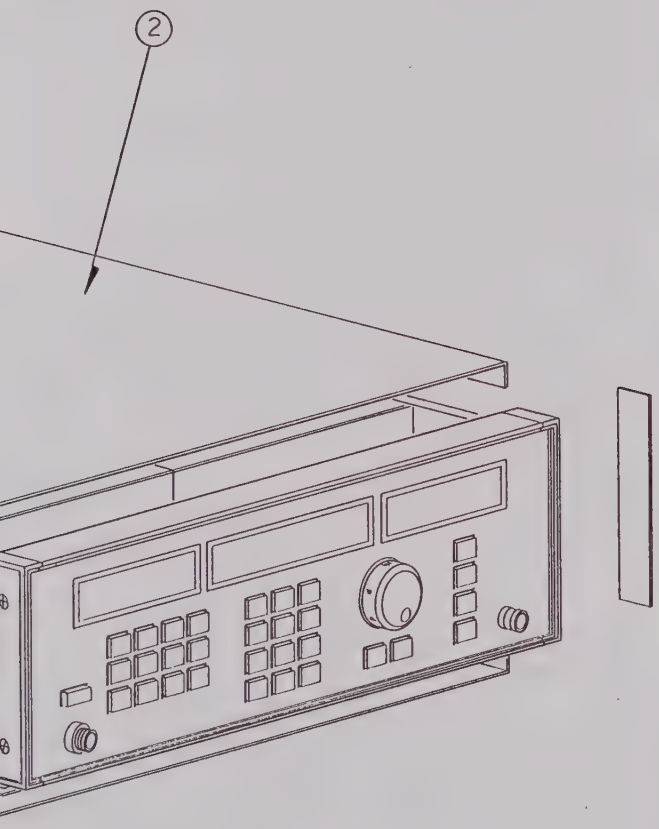


NOTE UNLESS OTHERWISE SPECIFIED



REFERENCE BOM *1111-00-0179

FIGURE 10-16B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN E. Walker	DATE 2/86	WAVETEK
MATERIAL	PROJ ENG	8/86	TITLE WRAP UP KIT — DRAWING —
	REL BY ENGR APPROV	8/1/86	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX XX ANGLES		
	DO NOT SCALE DWG		MODEL NO 2500 / DWG NO. 0012-30-0033 / REV
	SCALE 1/2		CODE IDENT 34280 / SHEET 2 OF 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
1	BOTTOM COVER AY,2500	2500-BOT CVR	W-I	1219-00-0598	1.000
2	TOP COVER,2500PER B/T	1410-80-1900	W-I	1410-80-1900	1.000
3	SEMS-PPH-INT 6-32X1/4,BK ZINC	PER DESC2810-58-6104	F-S	2810-58-6104	4.000
4	HANDLE END CAP,2500 PER B/P	1410-01-4720	W-I	1410-01-4720	4.000
5	SIDE DRESS DECAL PER B/P	1400-01-9370	WSD	1410-30-7430	2.000
6	BOTTOM SHIELD,2500 PER B/P	1410-60-3560	W-I	1410-60-3560	1.000
7	SIDE TRIM PIECE,2500 PER B/P	1410-80-1890	W-I	1410-80-1890	2.000
8	CABLE CLAMP,SELF-AD .56X.20	KKF-10X4	RICH	2810-00-0026	4.000
9	HANDLE	8002-529-LESS END CA	PHC	2810-07-0013	2.000
10	SCW,PDH,10-32X5/8,BK	19287-BK OXIDE	F-S	2810-64-0110	4.000
11	SCW,PPH,6-32X5/8,BK	19047-BK OXIDE	F-S	2810-65-6110	8.000
12	SEMS PPH-INT 4-40 X 1/4 NPPER B/P	PER DESC2810-57-4104	F-S	2810-57-4104	12.000
13	REAR SIDE RAIL FOOT PER B/P	1410-30-5090	W-I	1410-30-5090	2.000

WAVETEK PARTS LIST	WRAP UP KIT,2500	1111-00-0179 PAGE: 1	C REV

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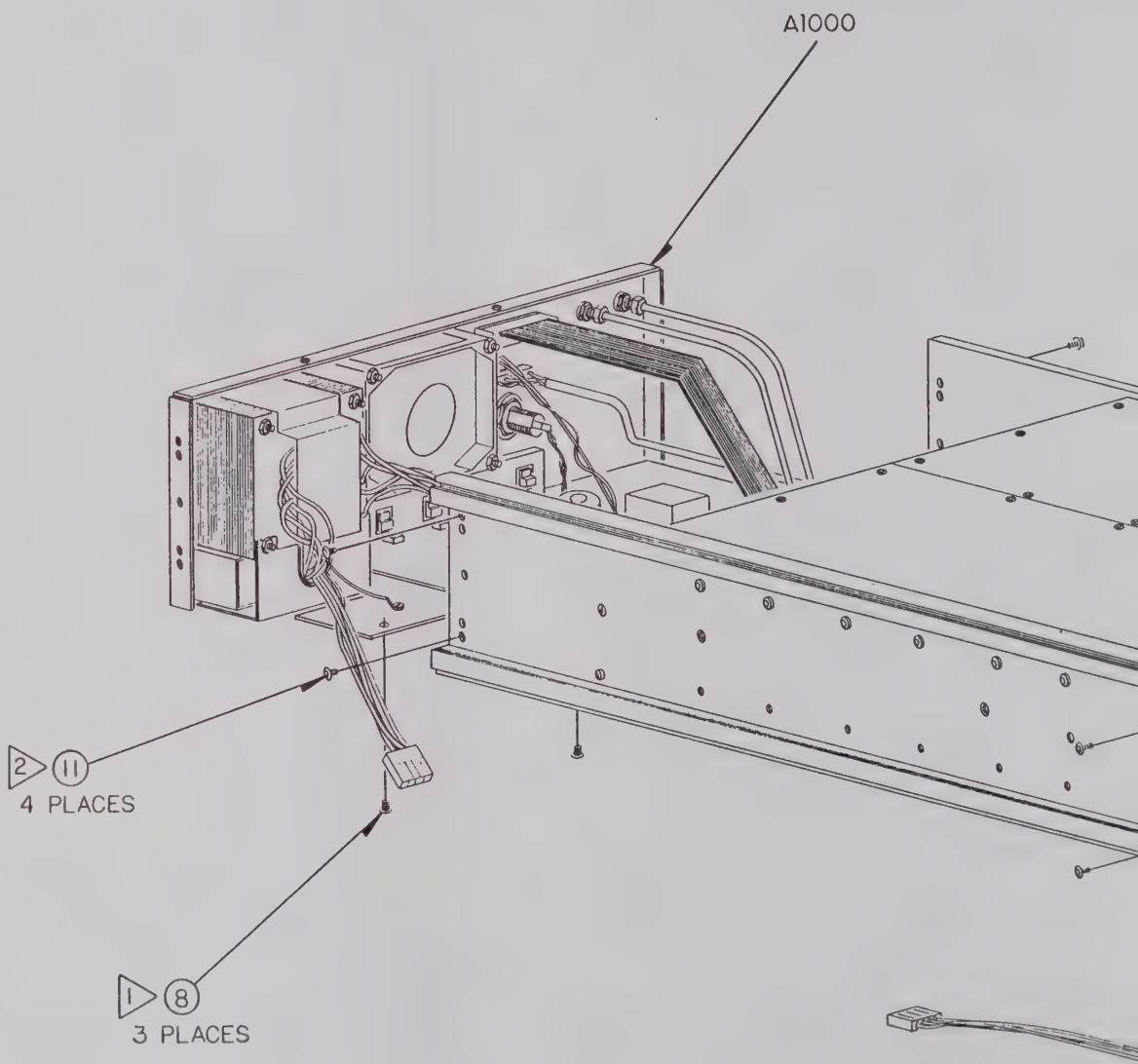
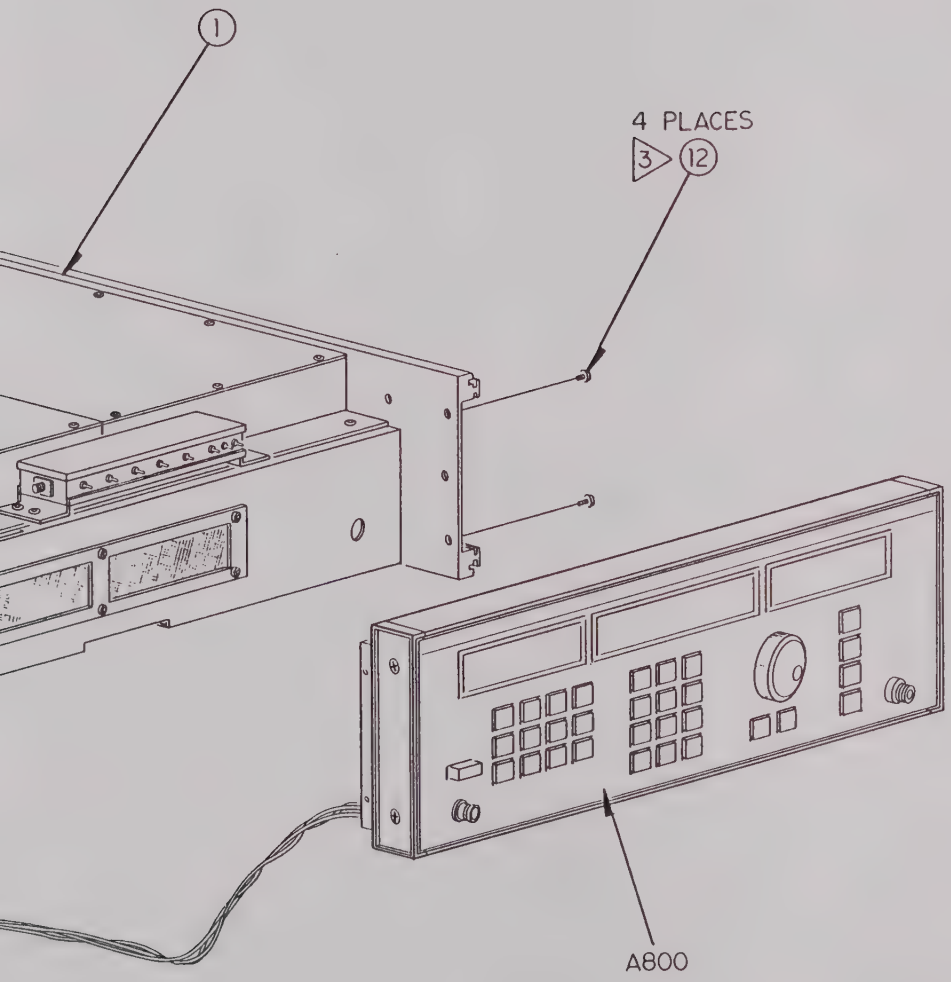


1 TORQUE TO 4.7 IN-LBS

2 TORQUE TO 8.7 IN-LBS

3 TORQUE TO 17.8 IN-LBS

NOTE UNLESS OTHERWISE SPECIFIED



REFERENCE BOM *1111-00-0178

FIGURE 10-17

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN E. Naylor	DATE 2/86	WAVETEK
MATERIAL	PROJECT	2/86	TITLE FINAL ASSY — DRAWING —
FINISH WAVETEK PROCESS	RELEASE APPROVAL	6/1/86	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX XX ANGLES		
	DO NOT SCALE DWG	MODEL NO. 2500	DWG NO. 0012-30-00
	SCALE 1/2	CODE IDENT 34280	SHEET 1

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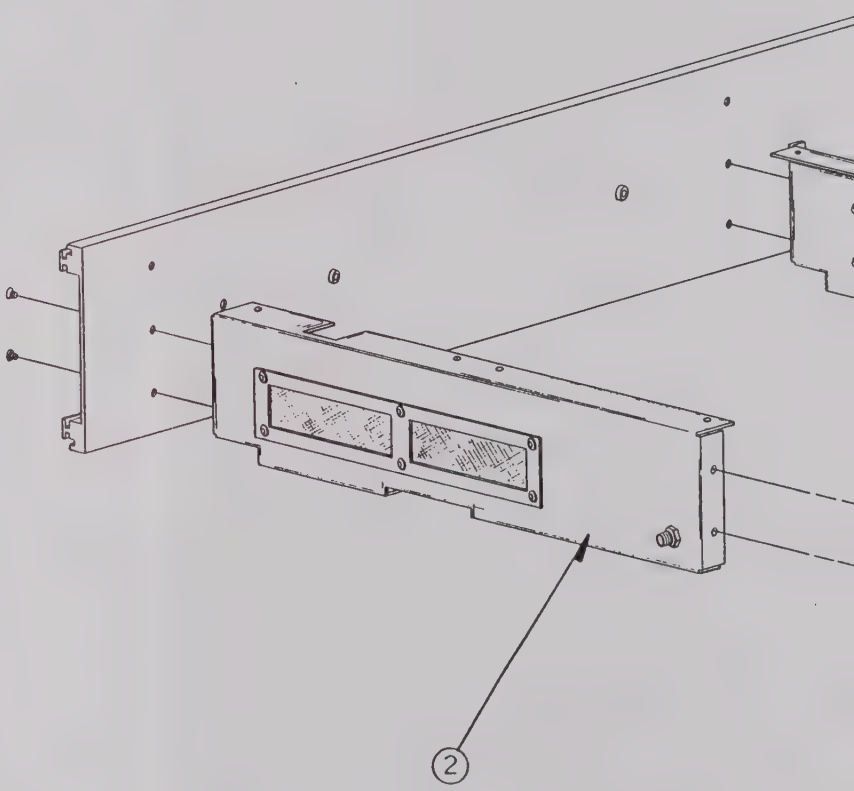
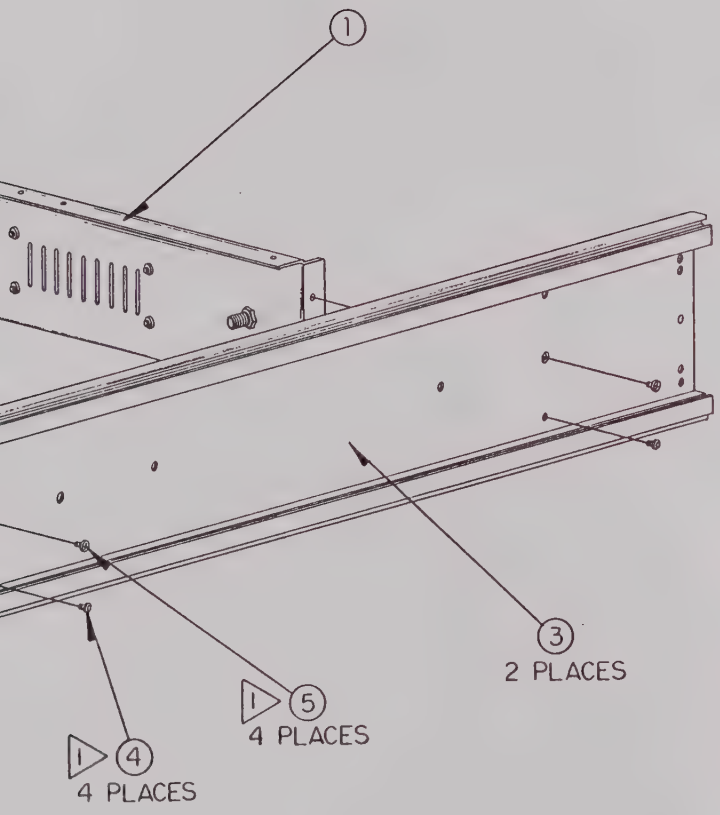


1 TORQUE TO 8.7 IN-LBS

NOTE UNLESS OTHERWISE SPECIFIED



REFERENCE BOM # 1111-00-0185

FIGURE 10-18

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. Naylor	DATE 1-86	WAVETEK
MATERIAL	PROJ ENGR		TITLE CHASSIS ASSY — DRAWING —
	RELEASE APPROV	2/11/86	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ANGLES .XX		
	DO NOT SCALE DWG		MODEL NO. 2500 / DWG NO. 0012-30-002
	SCALE 1/2		CODE IDENT 34280 / SHEET 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
1	MIDSECTION ASSY,2500	2500-MID SECTION	W-I	1110-00-2290	1.000
8	SCW,82 PFUCUT, 4-40X1/4	PER DESC2810-23-0092	F-S	2810-23-0092	3.000
11	SEMS-PPH-INT 6-32 X 1/4 NPPER B/P	PER DESC2810-57-6104	F-S	2810-57-6104	4.000
12	SEMS-PPH-INT 8-32 X 1/4 NPPER B/P	PER DESC2810-57-8104	F-S	2810-57-8104	4.000
A800	F.PANEL ASSY,2500	2500-FP ASSY	W-I	1110-00-2210	1.000
A1000	POWER SUPPLY,DPS2F, 2500	DPS2F-PS BD	W-I	1115-00-0045	1.000

WAVETEK PARTS LIST	FINAL ASSY,2500	1111-00-0178 PAGE: 1	C REV

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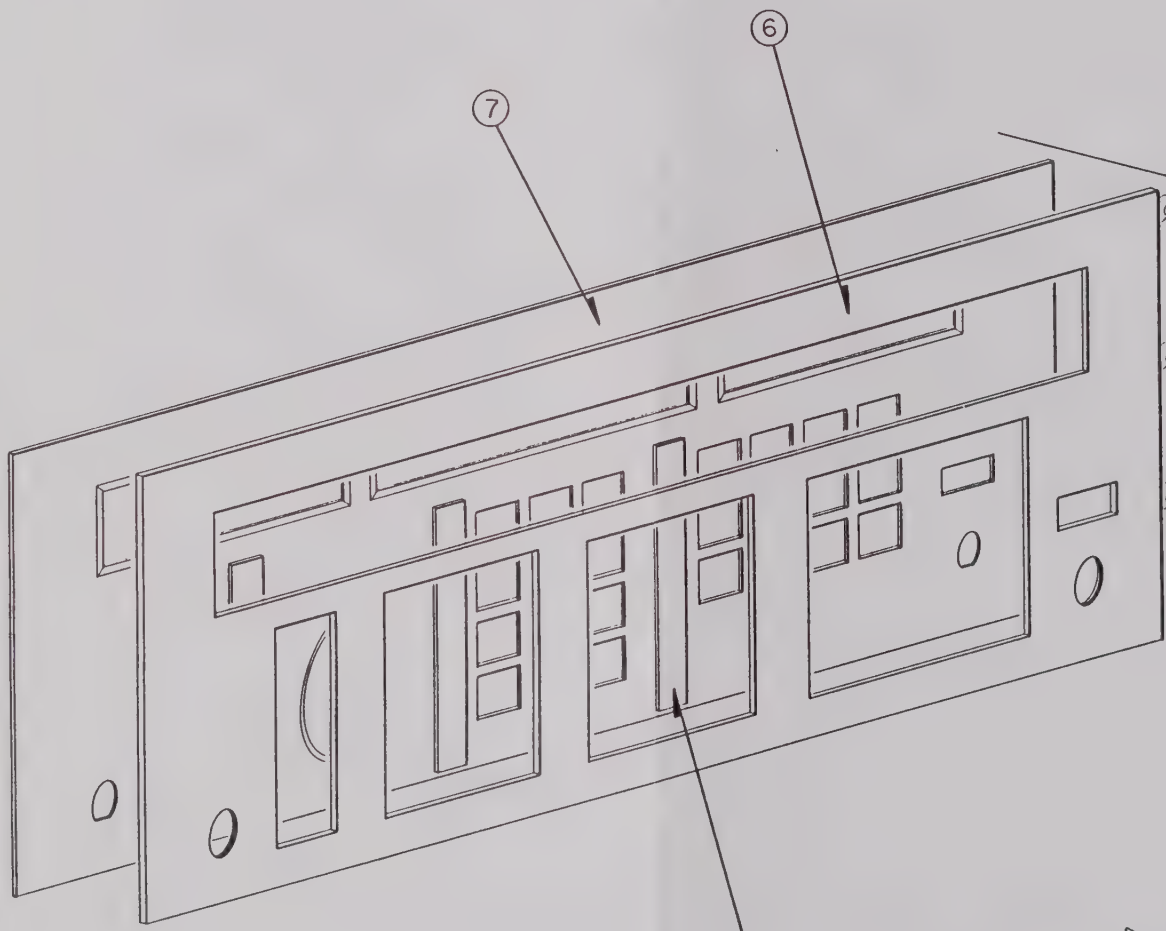
NOTE:

A FIXTURE IS USED TO ALIGN THE SPACER PANEL ⑥ AND DRESS PANEL ⑦



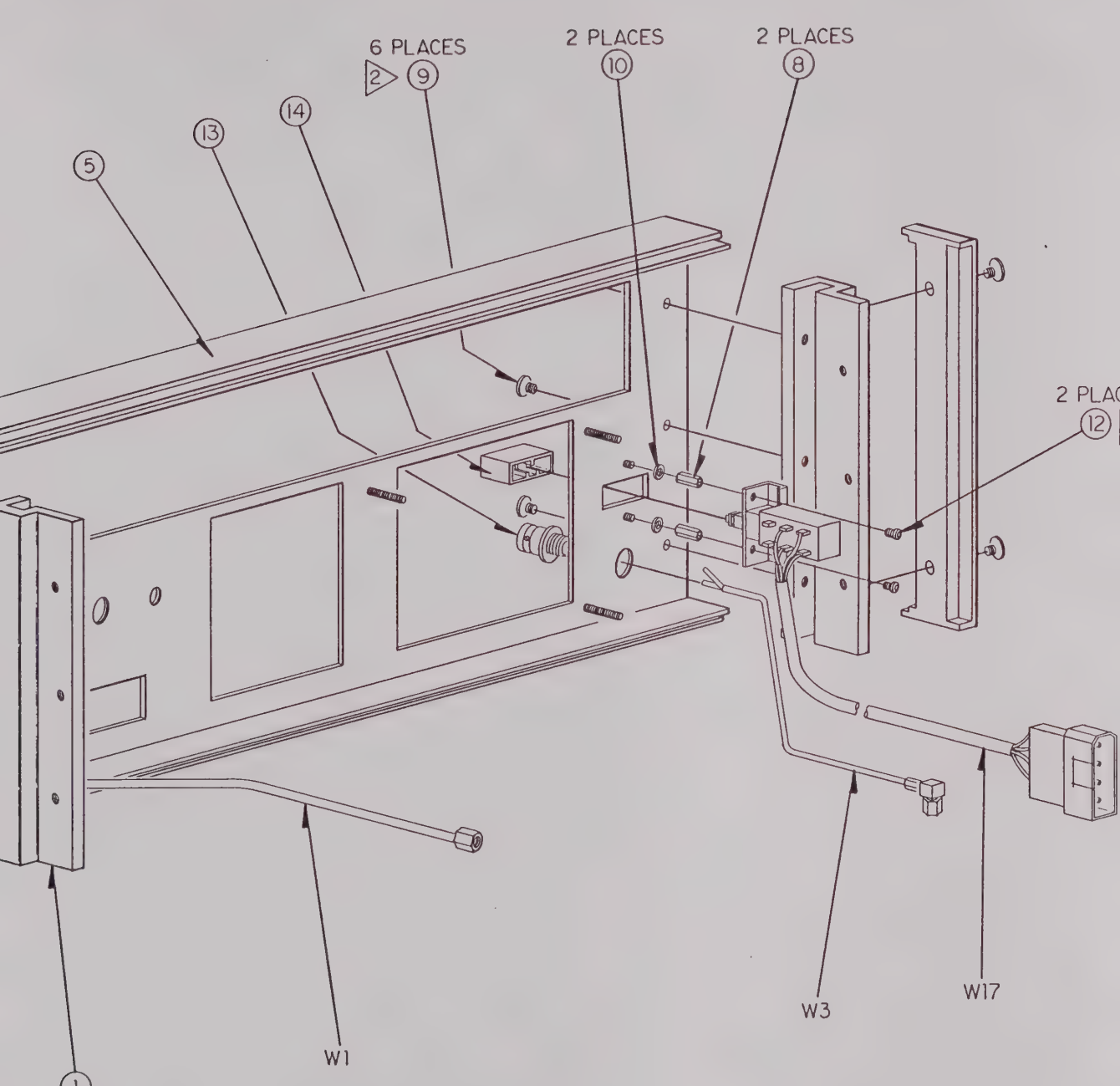
1 TORQUE TO 17

2 TORQUE TO 8

3 TORQUE TO 4

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY



REFERENCE BOM # 1216-00-0224

FIGURE 10-19

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. NAYLOR	DATE 1-86	WAVETEK
MATERIAL	PROJECTION		TITLE FRONT PANEL MECHANICAL ASSY — DRAWING —
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ANGLES .XX		
	DO NOT SCALE DWG	MODEL NO. 2500	DWG NO. 0012-30-00
	SCALE FULL	CODE IDENT 34280	SHEET 1

REFERENCE DESIGNATORS	PART DESCRIPTION >	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
1	REAR FIREWALL ASSY, 2500	2500-REAR FIREWALL	W-I	1216-00-0283	1.000
2	FRONT FIREWALL ASSY, 2500	2500-FRONT FIREWALL	W-I	1216-00-0284	1.000
3	2500 SIDE PANELS PER B/P FROM:3210-06-0010	1410-80-1870	W-I	1410-80-1870	2.000
4	SEMS-PFH-INT 6-32 X 1/4 NPPER B/P	PER DESC2810-57-6104	F-S	2810-57-6104	4.000
5	SCW,B2 PFUCUT, 6-32X1/4	PER DESC2810-23-0096	F-S	2810-23-0096	4.000

WAVETEK PARTS LIST	CHASSIS ASSY,2500	1111-00-0185 PAGE: 1	1 REV

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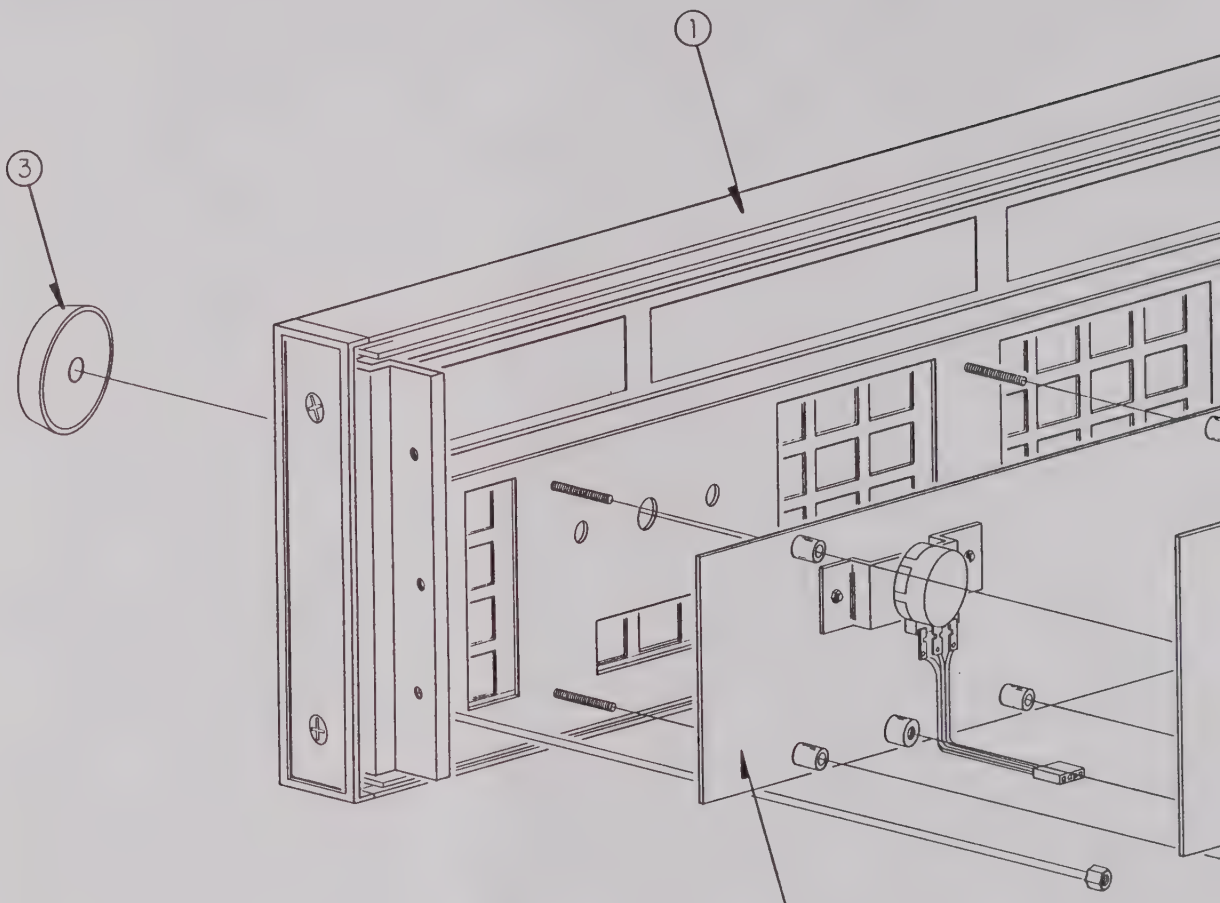
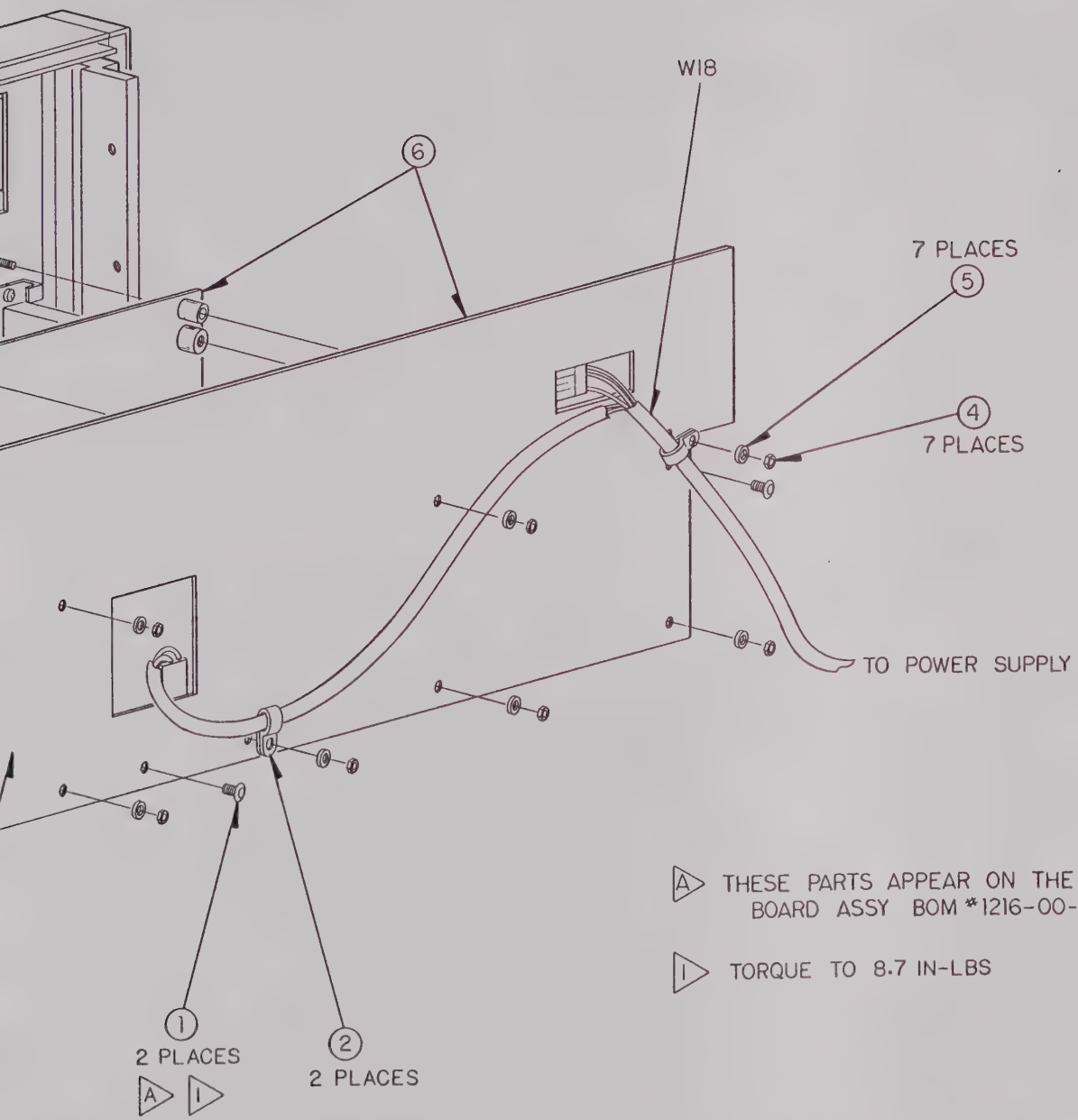


NOTE UNLESS OTHERWISE SPECIFIED



A THESE PARTS APPEAR ON THE KEY/DISPLAY BOARD ASSY BOM *1216-00-0286

1 TORQUE TO 8.7 IN-LBS

REFERENCE BOM *1110-00-2210

FIGURE 10-20

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. NAYLOR	DATE 1-86	WAVETEK
MATERIAL	PROJ ENGR		TITLE FRONT PANEL ASSY — DRAWING —
	RELEASE APPROV	8/1/86	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ANGLES .XX		
	DO NOT SCALE DWG	MODEL NO. 2500	DWG NO. 0012-30-002
	SCALE FULL	CODE IDENT 34280	SHEET 1

4 3 2 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
1	FP MECHANICAL ASSY, 2500	2500-FP MECH	W-I	1216-00-0224	1.000
2	CABLE CLAMP,3/16	F2NY-187NA	WHBRY	2810-00-0008	2.000
3	KNOB	1201-00-1731	WSD	2410-01-0073	1.000
4	NUT,4-40,HN101-400	8002A-NP	F-S	2810-14-4100	7.000
5	LO,WASHER,INT,4 HW101-400	1331NP	F-S	2810-24-4000	7.000
6	KEY/DISPLAY BD ASSY, 2500	2500-KEY/DISPLAY	W-I	1216-00-0286	1.000
W1B	BACKLIGHT CABLE,2500	WY2500-W1B	W-I	1219-00-0604	1.000

WAVETEK PARTS LIST	F.PANEL ASSY,2500	1110-00-2210 PAGE: 1	B REV

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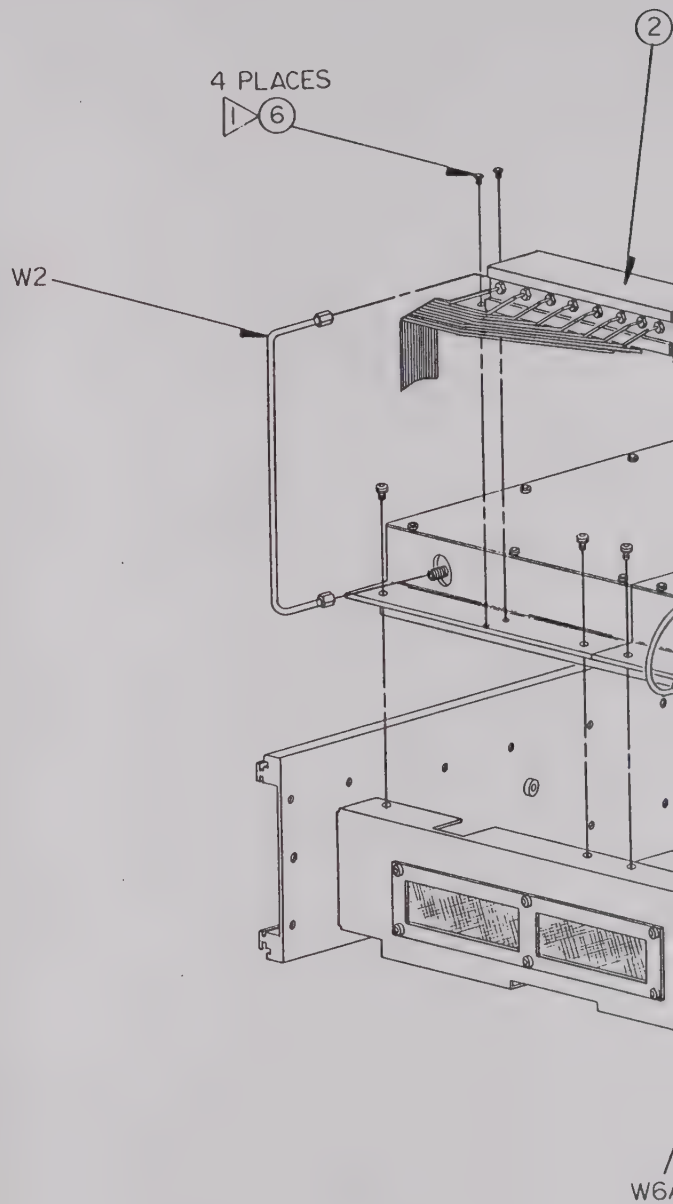


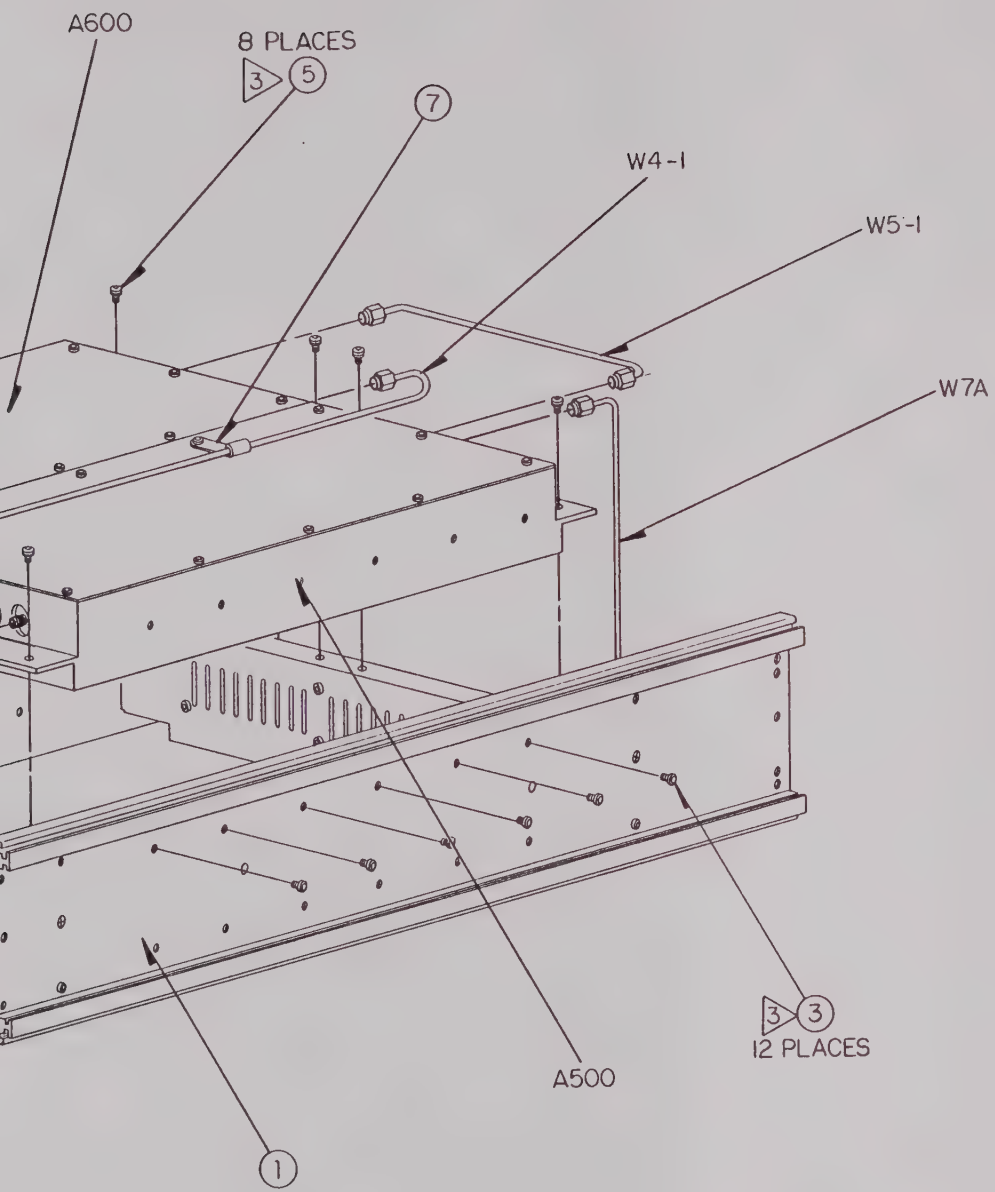
1 TORQUE TO 12 IN-LBS

2 TORQUE TO 4.7 IN-LBS

3 TORQUE TO 8.7 IN-LBS

4 TIGHTEN SNUG BY HAND ONLY

NOTE UNLESS OTHERWISE SPECIFIED



REFERENCE BOM # 1110-00-2290

FIGURE 10-21A

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B.Hoffner	DATE 1-86	WAVETEK
MATERIAL	PROFENGR D.L.O.	8/86	TITLE MID-SECTION ASSY — DRAWING —
	RELEASE AUTHON K.W.	8/14/86	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ANGLES .XX		
	DO NOT SCALE DWG	SCALE 1/2	MODEL NO. 2500 DWG NO. 0012-30-0027
			CODE IDENT 34280 SHEET 1

4 3 2 1

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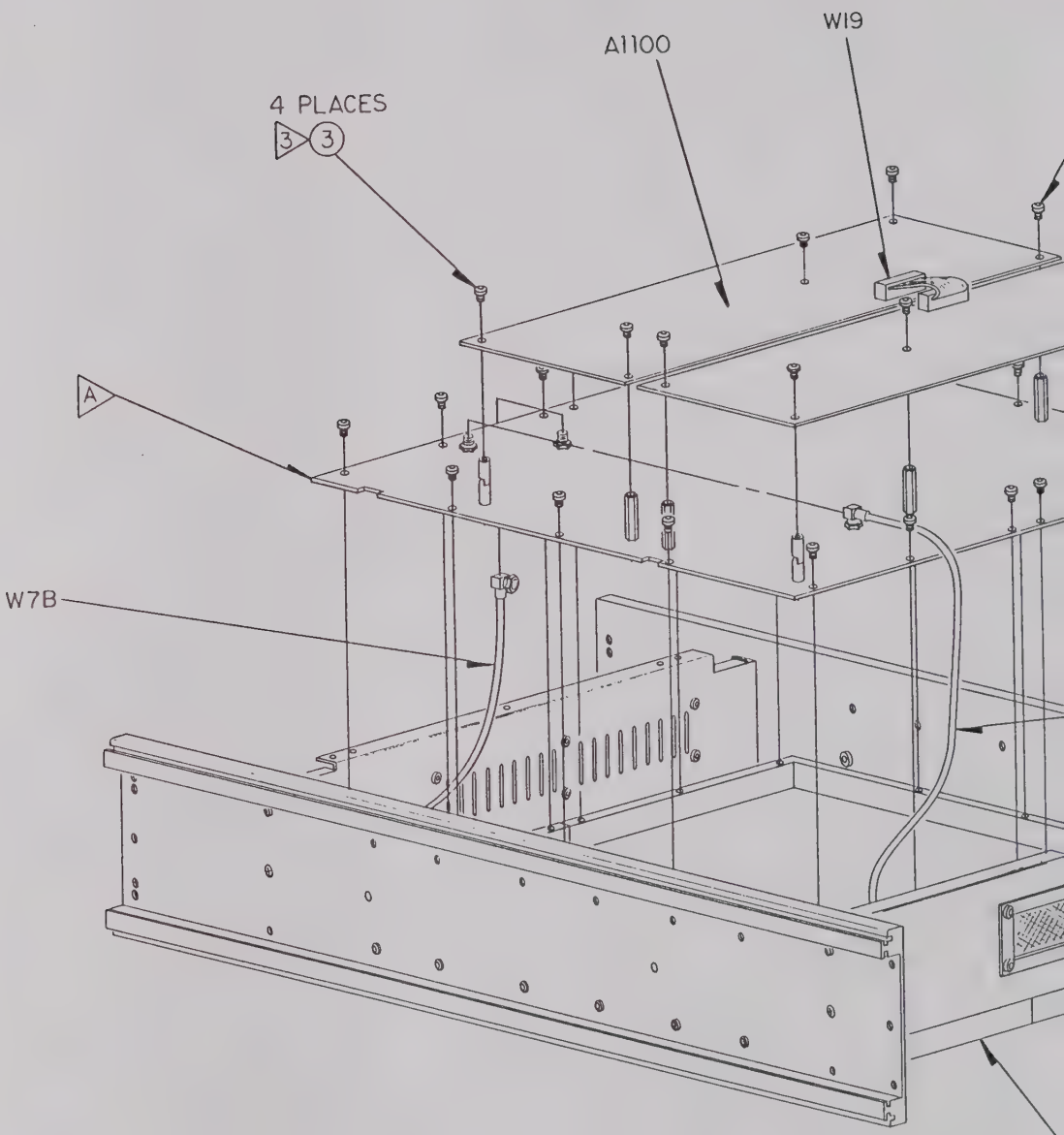
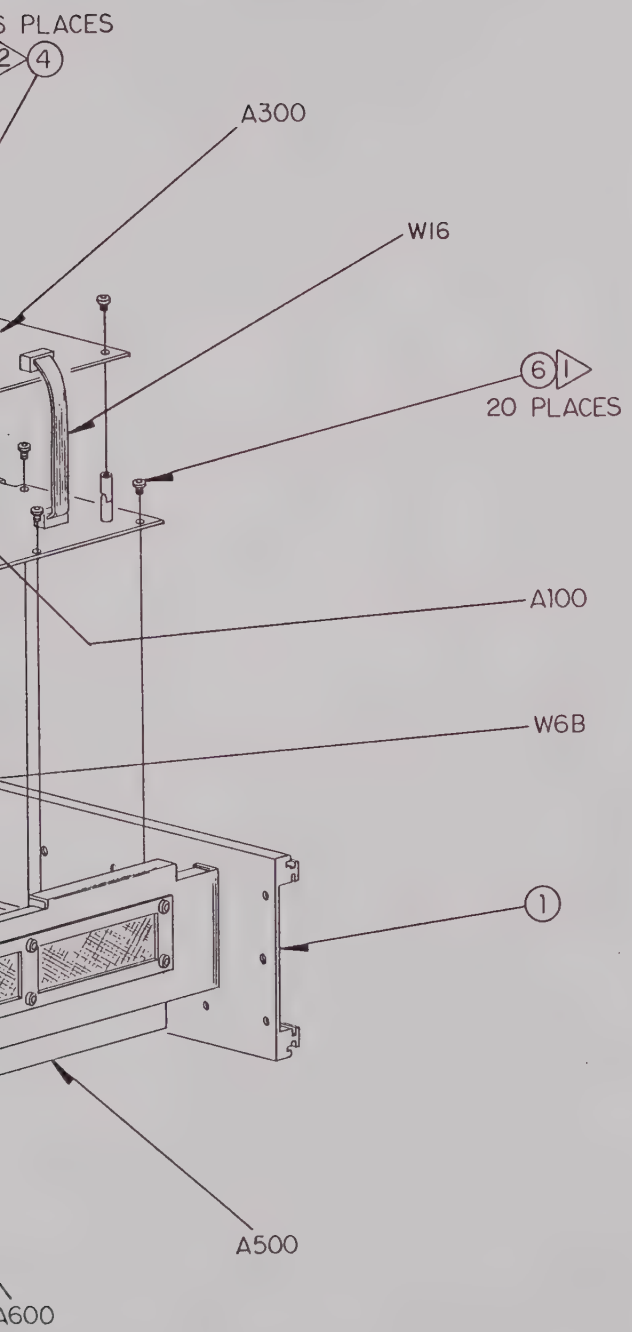


A CAUTION : USE EXTREME CARE WHEN ALIGNING AND INSERTING MAIN BOARD CONNECTORS TO AMP AND VCO CONNECTORS. FEEDTHRU CAPS ARE VERY FRAGILE.

NOTE UNLESS OTHERWISE SPECIFIED

8	7	6	5



REFERENCE BOM #1110-00-2290

FIGURE 10-21B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. Naylor	DATE 8/88	WAVETEK
MATERIAL	PROJ. ENGR.		TITLE MID-SECTION ASSY — DRAWING
	RELEASE APPROV.	8/88	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ANGLES XX		
	DO NOT SCALE DWG		MODEL NO. 2500 / DWG NO. 0012-30-0023 / REV
	SCALE 1/2		CODE IDENT 34280 / SHEET 2 OF 2

4 3 2 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
1	CHASSIS ASSY,2500	2500-CHAS	W-I	1111-00-0185	1.000
2	ATTEN ASSY, 2500	2500-ATTEN ASSY	W-I	1219-00-0607	1.000
3	SEMS-PPH-INT 6-32 X 1/4 NPPER B/P	PER DESC2810-57-6104	F-S	2810-57-6104	16.000
4	SEMS-PPH-INT 4-40 X 1/4 NPPER B/P	PER DESC2810-57-4104	F-S	2810-57-4104	6.000
5	SEMS-PPH-INT 6-32 X 3/8 NPPER B/P	PER DESC2810-57-6106	F-S	2810-57-6106	8.000
6	4-40X3/8 PPH,THREAD FORMING,ZP STEEL, SELF LOCKING	2810-23-0136PER DESC	ELCO	2810-23-0136	24.000
7	CABLE CLAMP,1/16	N-1	RICH	2810-00-0014	1.000
A100	MAIN BD ASSY,2500	2500-MAIN BD	W-I	1110-00-2240	1.000
A300	UPROC BD ASSY,2500	2500-UPROC BD	W-I	1110-00-2250	1.000
A500	OSCILLATOR ASSY,2500	2500-OSC ASSY	W-I	1110-00-2220	1.000
A600	AMPLIFIER ASSY,2500	2500-AMP ASSY	W-I	1110-00-2230	1.000
A1100	GPIB BD,2500	2500-GPIB	W-I	1019-00-0271	1.000
SCH	SCH,VCO BD,2500	0014-30-0355	W-I	0014-30-0355	1.000
W02	CABLE ASSY, 3.5 IN	WX2500-W2	W-I	1217-90-0120	1.000
W4-1	CABLE ASSY,17.5 IN	WX2500-W4	W-I	1217-90-0122	1.000
W5-1	CABLE ASSY,7.5 IN	WX2500-W5	W-I	1217-90-0121	1.000
W6A	CABLE ASSY, 5 IN	WX2500-W6A	W-I	1217-80-0124	1.000
W6B	CABLE ASSY,15.5 IN	WX2500-W6B	W-I	1217-80-0122	1.000
W7A	CABLE ASSY, 6 IN	WX2500-W7A	W-I	1217-80-0123	1.000
W7B	CABLE ASSY,5 IN	WX2500-W7B	W-I	1217-80-0121	1.000
W16	MAIN BD JUMPER CABLE 2500	WY2500-W16	W-I	1219-00-0603	1.000
W19	JUMPER CABLE,2500	WY2500-W19	W-I	1219-00-0605	1.000

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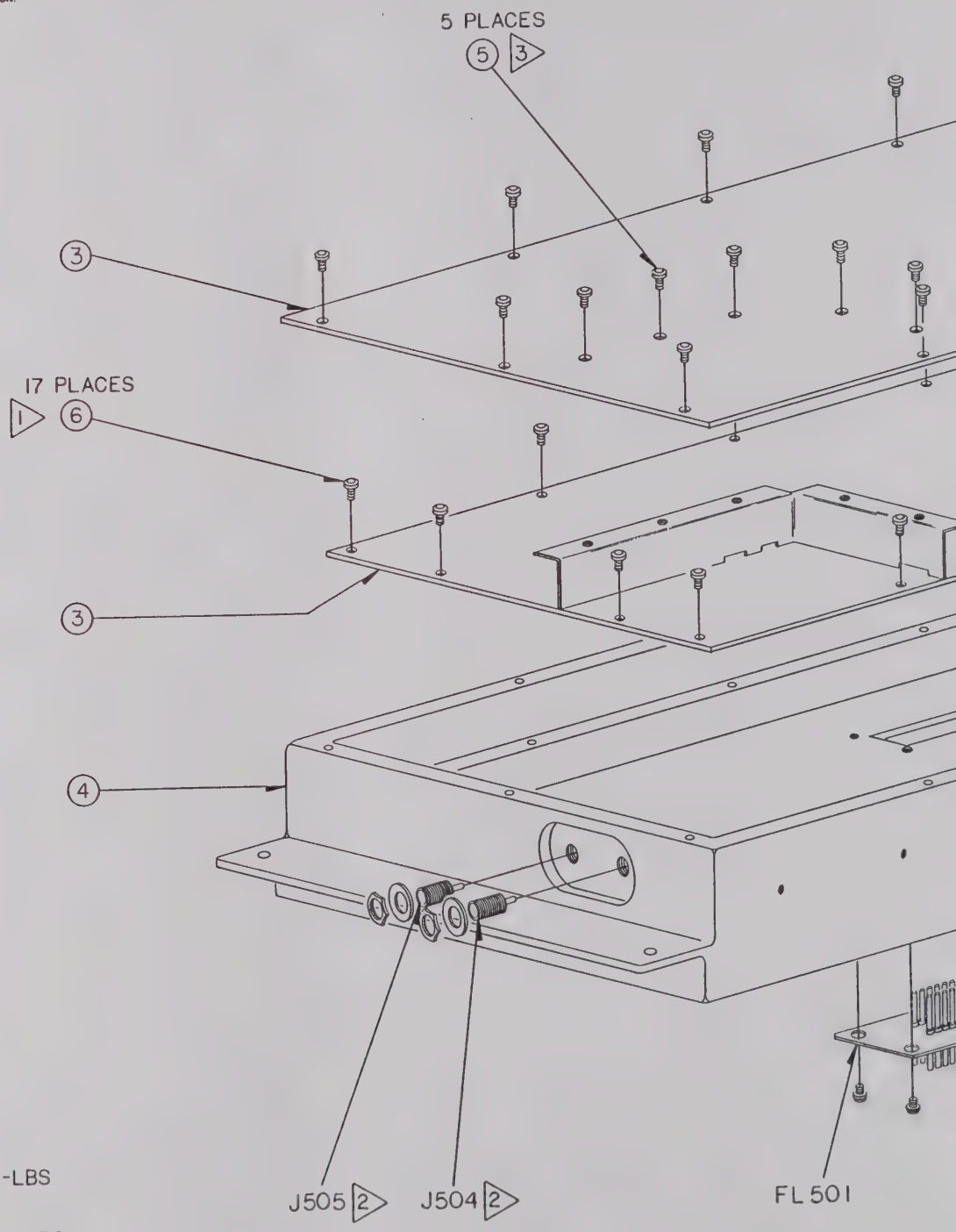
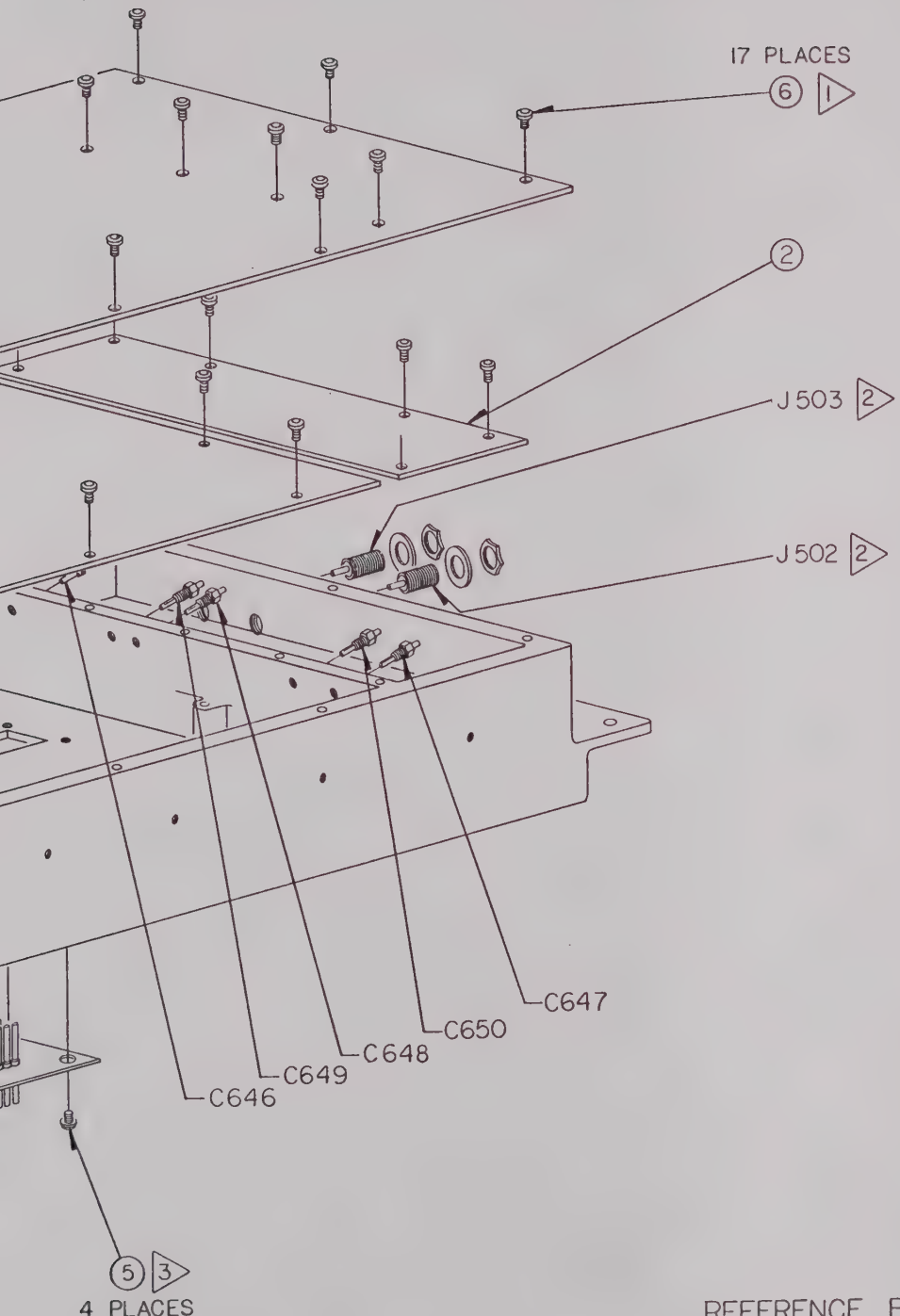


1 TORQUE TO 12 IN-LBS

2 TORQUE TO 25 IN-LBS

3 TORQUE TO 4.7 IN-LBS

NOTE UNLESS OTHERWISE SPECIFIED



REFERENCE BOM *1110-00-2210

FIGURE 10-22

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE 6/82	WAVETEK
MATERIAL	PROGENCY	8/82	TITLE OSCILLATOR ASSY — DRAWING —
	RELEASE APPROVED	8/1/84	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ANGLES .XX		
	DO NOT SCALE DWG	MODEL NO. 2500	DWG NO. 0012-30-00
	SCALE FULL	CODE IDENT 34280	SHEET 1

4	3	2	1

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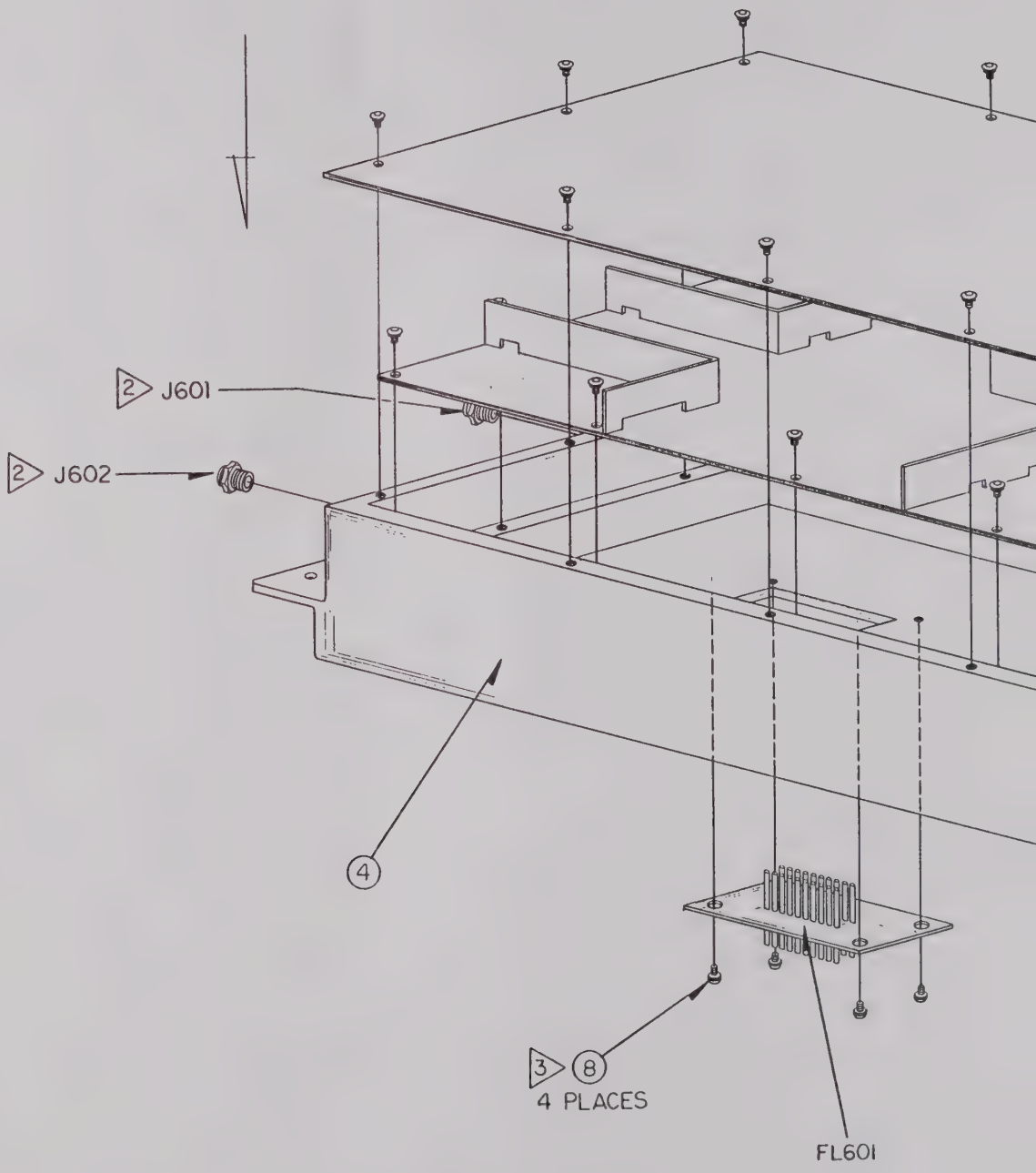
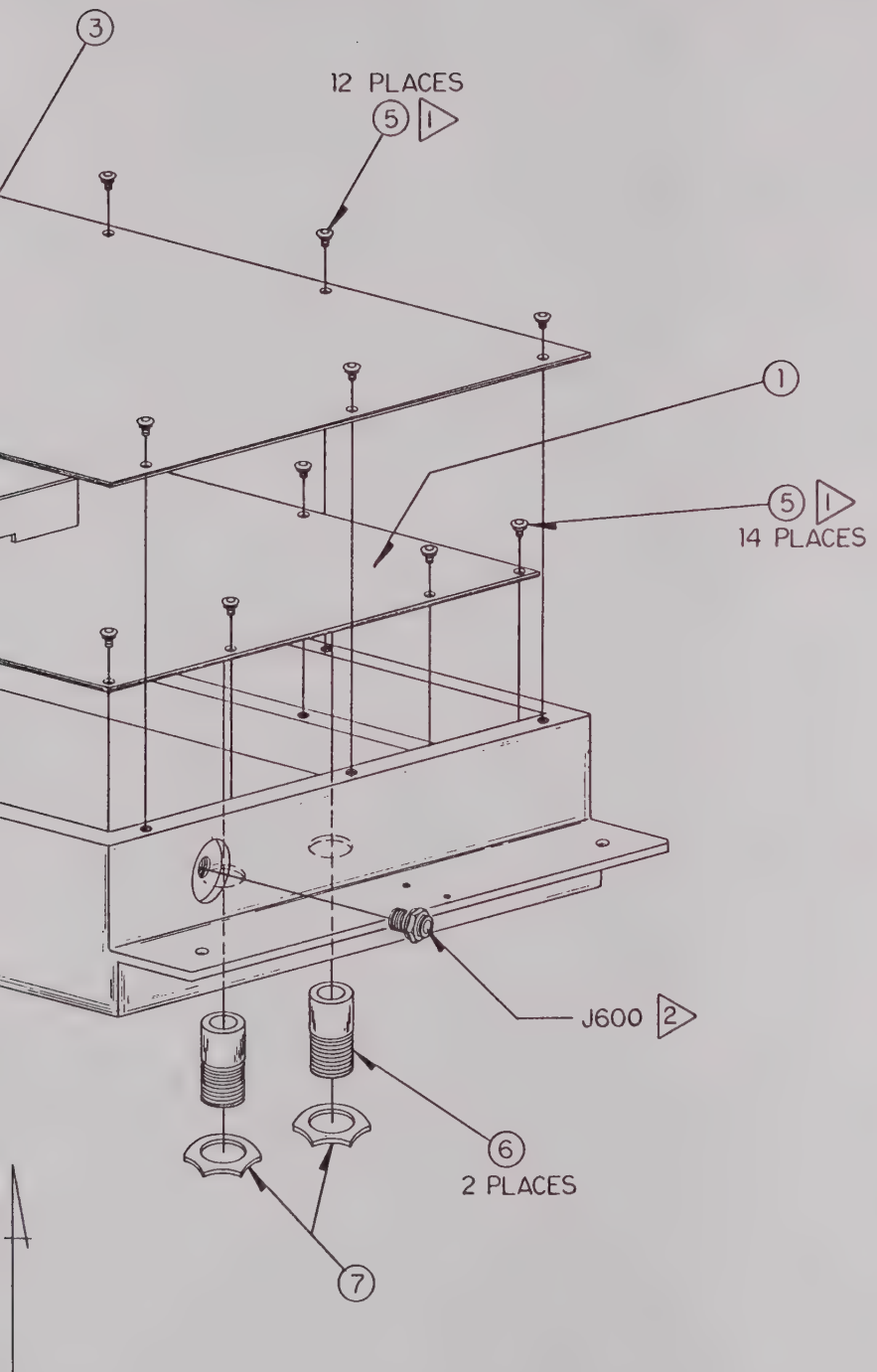


1 TORQUE TO 12 IN-LBS

2 TORQUE TO 25 IN-LBS

3 TORQUE TO 4.7 IN-LBS

NOTE UNLESS OTHERWISE SPECIFIED



REFERENCE BOM # 1110-00-2230

FIGURE 10-23

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B Norton DATE 1-86	WAVETEK	
MATERIAL	PROJ ENGR 2/84	TITLE AMPLIFIER ASSY — DRAWING —	
	RELEASE APPROV 8/1/84		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ANGLES .XX		
	DO NOT SCALE DWG	MODEL NO. 2500	DWG NO. 0012-30-00
	SCALE FULL	CODE IDENT 34280	SHEET 1

4	3	2	1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
1	OSCILLATOR BD,2500	2500-OSC BD	W-I	1218-00-2290	1.000
2	LOCAL OSC BD, 2500	2500-LOCAL OSC BD	W-I	1218-00-2590	1.000
3	VCO,COVERPER B/P	1410-60-3780	W-I	1410-60-3780	1.000
4	VCO MODULE CAVITY, PER B/P REF:1410-80-2120	1410-80-1940	W-I	1410-80-1940	1.000
5	SEMS-PPH-INT 4-40 X 3/16 NFPER B/P	PER DESC2810-57-4103	F-S	2810-57-4103	9.000
6	4-40X3/8 PPH,THREAD FORMING,ZP STEEL, SELF LOCKING	2810-23-0136PER DESC	ELCO	2810-23-0136	34.000
7	ST SCREW,CONE,SKT, 4-40X3/8,BLK.OX.	SS-4-40X3/8,CONE	F-S	2810-43-4106	4.000
8	VCO CASTING FOAM CVR 2500A	1410-60-3980	W-I	1410-60-3980	1.000
C646 C647 C648 C649 C650	FILTER,EMI,15 AMP	859619-1	AMP	2710-01-0004	5.000
FL501	VCO MOD EMI FILTER, 2500	2500-VCO MOD FILTER	W-I	1219-00-0596	1.000
J502 J503 J504 J505	CONN,SMA-F,50,PANEL	2058-5029-02	O-S	2110-02-1020	4.000

WAVETEK PARTS LIST	OSCILLATOR ASSY,2500	1110-00-2220 PAGE: 1	E REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY
1	AMPLIFIER BD,2500	2500-AMP BD	W-I	1218-00-2300	1.000
2	RF CASTING FOAM CVR 2500A	1410-60-3990	W-I	1410-60-3990	1.000
3	VCO & RF MOD COVER, 2500PER B/P	1410-60-3540	W-I	1410-60-3540	1.000
4	RF MOD CAVITY,2500 PER B/P REF:1410-80-1800	1410-80-1950	W-I	1410-80-1950	1.000
5	4-40X3/8 FPH,THREAD FORMING,ZP STEEL, SELF LOCKING	2810-23-0136PER DESC	ELCO	2810-23-0136	26.000
6	HEATSINK FOR AMP BD PER B/P	1410-01-4880	W-I	1410-01-4880	2.000
7	HEX,NUT,1/2-28 HN111-001	17-220NP	F-S	2810-16-0003	2.000
8	SEMS-PPH-INT 4-40 X 1/4 NPPER B/P	PER DESC2810-57-4101	F-S	2810-57-4104	4.000
9	ST SCREW,CONE,SKT, 4-40X3/8,BLK.OX.	SS-4-40X3/8,CONE	F-S	2810-43-4106	3.000
FL601	RF MOD EMI FILTER, 2500	2500-RF MOD FILTER	W-I	1219-00-0397	1.000
J600 J601 J602	CONN,SMA-F,50,PANEL	2058-5029-02	O-S	2110-02-1020	3.000
KIT	TECH KIT, AMP ASSY, 2500	2500-TECH KIT-AMP	W-I	1219-00-0611	1.000

MP MASTER
MA35438